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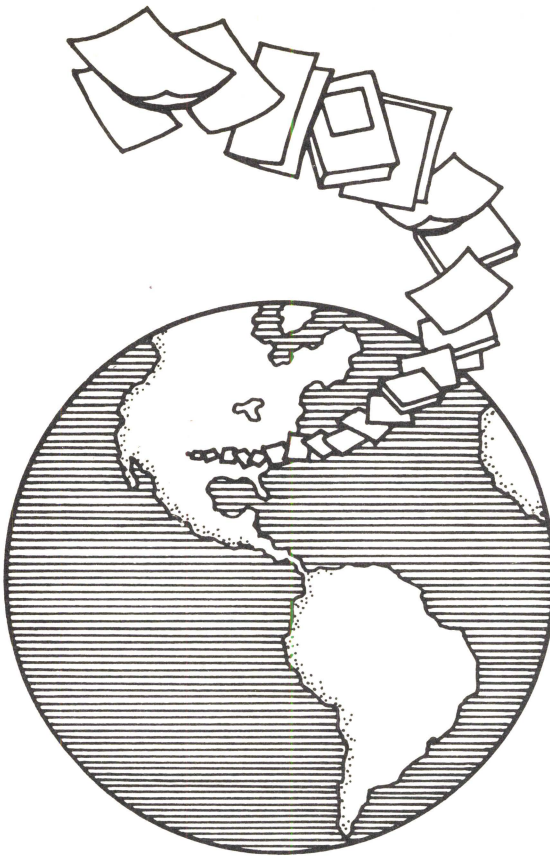
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1987

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## INTRODUCTION

Intel introduced the first microprocessor in 1971. Today, microprocessors touch all our lives from factories to fields, and from our offices to our homes. The microelectronic revolution has brought greater productivity to industry, while it spawned new markets and businesses, and contributed to higher quality products and a better life. As we approach the 1990's, microprocessors continue to trigger a worldwide information revolution. Personal computers, communications networks, and advances in software are providing the productivity tools necessary in today's complex office and industrial environments. In this issue Intel is acknowledging the important part that communication networks and components play on the needs of PC communication.

Intel, as the founder of microprocessor development, is dedicated to the use of microprocessors in all industries. We develop microprocessors, microcontrollers, communication components, memory components, boards, software, and integrated systems products. All these products are based on "Open Standards" and "Open Systems" that allow you to use our components, boards, software, or systems to meet your needs quickly and produce reliable products for your market. This Product Guide summarizes Intel's complete offering of our products and services.

In this issue, Intel's Microcommunications section is dedicated to the communications products, both components, boards and systems which provide quick-time-to-market solutions to today's multivendor office and industrial environments.

## HOW TO USE THIS GUIDE

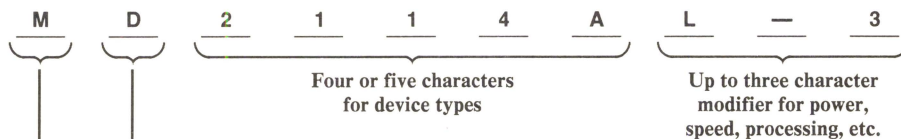
Intel offers this Product Guide as a ready reference "tool" to make it easy for you to select the set of products you'll need to meet your design objectives. You won't find every performance parameter for every device here, but you will find key features, and more importantly, cross references to products required for "total solution" designs. Products are arranged in family groups and are shown in tabular form so you can find what you need fast. Footnotes will guide you to related products. An Alphanumeric Index is located on Page viii to point you directly to the page where each product is listed. In the Product Highlights we've provided a few examples of how particular designs can be executed using Intel products. Military and EXPRESS program (extended reliability) components are recapped in special sections. Customer Support Services are also contained in the Guide, and include Customer Training, Consulting, and Software and Hardware Support.

## WHERE TO FIND MORE INFORMATION

For complete product line data sheets, application notes, etc., refer to the appropriate Intel handbooks listed on the inside front cover of the Guide or consult the Intel Literature Guide. For additional assistance, call your local Intel Sales Office or distributor listed in the last section of this Guide.

## PRODUCT IDENTIFICATION CODE

Semiconductor components are identified as follows:



### Package Type

- A — Ceramic, Pin Grid Array
- B — Hermetic Package, Type B
- C — Hermetic Package, Type C (Ceramic)
- D — Hermetic Package, Type D (Cerdip)
- L — Laminated Plastic
- N — Plastic Leaded Chip Carrier (PLCC)
- P — Plastic Package
- R — Hermetic, Leadless Chip Carrier (LCC)
- V — Plastic Leaded Chip Carrier
- X — Unpackaged Device

M — Indicates Military Operating Temperature Range

I — Indicates Industrial Grade

J — Indicates a JAN qualified device, but is for internal identification purposes only. All JAN devices must be ordered by M38510 part number (Example: M38510/42001 BQB), and will be marked in accordance with MIL-M-38510 specifications.

L — Indicates extended operating temperature range ( $-40^{\circ}\text{C}$  to  $-85^{\circ}\text{C}$ ) Express product with  $168 \pm 8$  hrs. dynamic burn-in.

Q — Indicates commercial temperature range ( $0^{\circ}\text{C}$  to  $-70^{\circ}\text{C}$ ) Express product with  $168 \pm 8$  hrs. dynamic burn-in.

T — Indicates extended temperature range ( $-40^{\circ}\text{C}$  to  $-85^{\circ}\text{C}$ ) Express product without burn-in.

### Examples:

D2147H-1 High Speed 4096 x 1-Bit Static RAM (35ns, 180/30 mA), hermetic package Type D.

C8080A2 8080A Microprocessor with 1.5  $\mu$ s cycle time, hermetic package Type C, commercial temperature range.

MD8080A/B 8080A Microprocessor, hermetic package Type D, military temperature range, MIL-STD-883 Level C processing.\*

\*On Military temperature devices, C suffix indicates MIL-STD-883 Level C processing.



## **CUSTOMER SUPPORT**

### **CUSTOMER SUPPORT**

Customer Support is Intel's complete support service that provides Intel customers with hardware support, software support, customer training, and consulting services. For further information contact your local Sales Office.

After a customer purchases any system hardware or software product, service and support become major factors in determining whether that product will continue to meet a customer's expectations. Such support requires an international support organization and a breadth of programs to meet a variety of customer needs. As you might expect, Intel's customer support is quite extensive. It includes factory repair services and worldwide field service offices providing hardware repair services, software support services, customer training classes, and consulting services.

### **HARDWARE SUPPORT SERVICES**

Intel is committed to providing an international service support package through a wide variety of service offerings available from Intel Hardware Support. See Table 1 for list of services.

### **SOFTWARE SUPPORT SERVICES**

Intel's software support consists of two levels of contracts. Standard support includes TIPS (Technical Information Phone Service), updates and subscription service (product-specific troubleshooting guides and ;COMMENTS Magazine). Basic support includes updates and the subscription service. Contracts are sold in environments which represent product groupings (i.e., iRMX environment). See Table 2 for a complete listing of environments.

### **SYSTEMS ENGINEERING SERVICES**

Intel provides field systems engineering services for any phase of your development or support effort. You can use our systems engineers in a variety of ways ranging from assistance in using a new product, developing an application, personalizing training, and customizing or tailoring an Intel product to providing technical and management consulting. Systems Engineers are well versed in technical areas such as microcommunications, real-time applications, embedded microcontrollers, and network services. You know your application needs; we know our products. Working together we can help you get a successful product to market in the least possible time.

### **CUSTOMER TRAINING**

Intel offers a wide range of instructional programs covering various aspects of system design and implementation. In just three to ten days a limited number of individuals learn more in a single workshop than in weeks of self-study. For optimum convenience, workshops are scheduled regularly at Training Centers worldwide or we can take our workshops to you for on-site instruction. Covering a wide variety of topics, Intel's major course categories include: architecture and assembly language, programming and operating systems, BITBUST<sup>™</sup> and LAN applications.

### **OEM, VAR, VEU SUPPORT SERVICES**

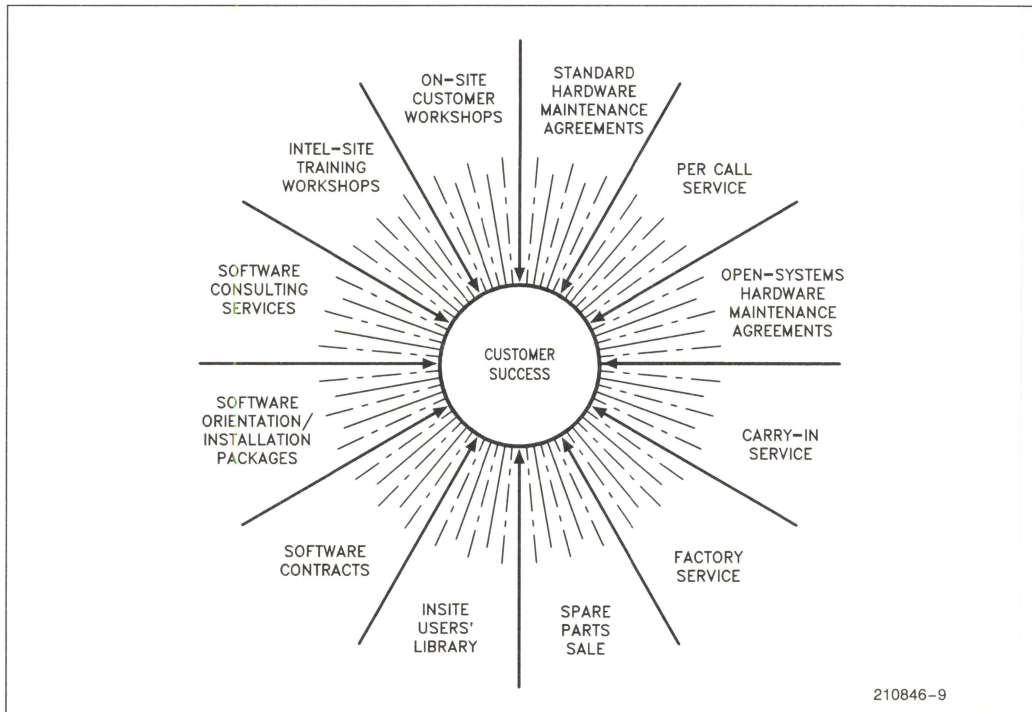
Our goal is to make your development easier and as productive as possible. Our support services are tailored to your specific needs whether they occur in the project start-up, development, or product introduction phase. The range of Intel support includes: on-site assistance from systems engineers for full-time project consulting; current software information with monthly bulletins and updates; preventative maintenance to keep important development equipment at its peak; access to product specialists, and technical training for your personnel. Through our Open Systems Support, we will also work with you to plan for your end-user support requirements by providing support for your entire system, not just the Intel portion—enhancing the marketability of your product.



## END-USER SUPPORT SERVICES

Our Smart Six Plan is the comprehensive way to get the most out of Intel's support. The plan consists of: 1) System Design, 2) Customer Training, 3) Installation, 4) Warranty, 5) Hardware/Software Support, and 6) Application Consulting. A team of System Engineers, hardware and software, and Network Specialists will work to custom design the best solution for even the most complex office environments.

## FULL RANGE OF SUPPORT SERVICES



**1-800-INTEL 4 U**  
**(1-800-468-3548)**

Our one "800" number nationwide accommodates all your support needs using centralized dispatch. Our one call/one number will get you to the right support you need: hardware, software, SBC repair, billing inquiries, and registration. Step-by-step instructions are provided when the "800" number is called.

**Table 1. Hardware Support Offerings**

Service	Highlights
Standard Hardware Maintenance Agreement	<ul style="list-style-type: none"> <li>• Full level service covering parts, labor, preventative maintenance and engineering change installations at the customer site.</li> <li>• Customer selects hours of coverage.</li> <li>• Applies to standard Intel products.</li> </ul>
Open Systems Support	<ul style="list-style-type: none"> <li>• Provides the international service capabilities on Intel's Hardware Support organization to the end-user customer of Systems Integrators and OEMs.</li> <li>• Individually tailored contracts to meet unique equipment configurations and customer support needs.</li> <li>• Usually includes support for non-Intel products as part of the total support agreement.</li> </ul>
Carry-in Maintenance Agreement	<ul style="list-style-type: none"> <li>• Economical</li> <li>• Same services as standard contract, but the customer delivers the equipment to an Intel facility.</li> </ul>
Per Call Services	<ul style="list-style-type: none"> <li>• Purchase labor and materials on an as-needed basis for installations, repairs, preventative maintenance, and other services.</li> </ul>
Factory Services Factory Direct Return Authorization Service (DRA)  Factory Return Replacement Authorization Service (RRA)	<ul style="list-style-type: none"> <li>• Economical 30-day turnaround</li> <li>• Applies to board level products in all areas and system customers in non-serviceable areas.</li> <li>• Expedited service 48-hour turnaround</li> <li>• Applies to currently manufactured board level products in minimal quantities.</li> </ul>
Installation	<ul style="list-style-type: none"> <li>• Included on many Intel system products. Customer Engineer installs, services and verifies correct operation before turning the system over to the customer.</li> </ul>
Warranty	<ul style="list-style-type: none"> <li>• Provided either via factory returns or at the customer site, depending on the warranty associated with that particular product.</li> </ul>

Not all services provided for all product lines. Contact your local Intel service office for more specific information on the right service to meet your needs.

**Table 2. Software Support Services**

Environment	Description
SSC 100/101	Eight-Bit Environment
SSC 200/201	Sixteen-Bit Environment (and S-III in Eight-Bit)
SSC 300/301	VAX/VMS* Resident Cross Software
SSC 400/401	iRMX® 86 Operating System
SSC 420/421	iRMX® 286 Operating System
SSC 500/501	XENIX** Operating System
SSC 510/511	iDIST™ Family (not including Host Comm)
SSC 520/521	iDIST™ Host Comm Family
SSC 600/601	Communication Network File Server Environments
SSC 700/701	DOS Environment

**NOTE:**

SSC 100, 200, 300, 400, 420, 500, 520, 600, 700: STANDARD SERVICE

SSC 101, 201, 301, 401, 421, 501, 521, 601, 701: BASIC SERVICE

\*VAX/VMS is a trademark of DEC Corp.

\*\*XENIX is a trademark of Microsoft Corp.

## CUSTOMER TRAINING WORKSHOPS

### Course Title

#### **INTRODUCTORY:**

Self Study Introduction to Microprocessors

Introduction to Microprocessors

#### **EMBEDDED CONTROLLERS:**

MCS®-51 Embedded Controllers

MCS®-96 16-Bit Embedded Controllers

MCS®-80/85 Embedded Controllers

80186, 80188 Embedded Controller

#### **MICROPROCESSORS:**

8086, 8088 Microprocessors Based Architecture

8086, 8088 Advanced Microprocessors

#### **BITBUS**

80286 Microprocessors

80386 Programming Using ASM 386

80386 System Software

#### **I<sup>2</sup>C™ USERS**

### Course Title

#### **MICROCOMPUTER PROGRAMMING & OPERATING SYSTEMS:**

Introduction to "C" Programming

System Programming in "C" for XENIX\*

PL/M Programming

PL/M-iRMX™ 51 Operating System

iRMX™ 86 Operating System Part I and II

iRMX 286 Operating System

iRMX™ Application & Debug

Fundamentals of XENIX

XENIX Shell Programming

XENIX System Administration

LAN Overview

iNA 960

iRMX-NET

LAN Applications/XENIX-NET

Office Automation

System Automation

Networks Administration

\*XENIX is a trademark of Microsoft Corp.





# COMPONENT QUALITY AND RELIABILITY

## INTEL CORPORATE QUALITY POLICY

It is the policy of Intel Corporation to design, manufacture, and deliver products that satisfy all our customer's expectations and perform reliably in their applications.

## CORPORATE QUALITY OVERVIEW AND CULTURE

Since the inception of the company, Intel has been recognized as an innovator and a leader in product quality & reliability—from silicon solutions to system products. This leadership was not achieved by accident. It resulted from a combination of clearly defined objectives, careful planning and thorough execution. At Intel "Quality" is a commitment, a philosophy, and a goal: a commitment to satisfy our customers' needs; a philosophy practiced as "do it right the first time" hinged on personal recognition that quality ownership rests on each individual; and a goal of excellence in the world marketplace.

## ORGANIZATION: AN EFFECTIVE QUALITY MATRIX

All Q & R organizations come under a uniform policy, while still maintaining the flexibility to service the specific needs of all product areas. To perform in this manner, a unique matrix organization has been developed. All Quality & Reliability functions report directly through Operations or Site Q & R Managers to the Director of Q & R for major policy and procedural matters. The flexibility is obtained by the Site/Operation QA Managers also reporting, in a matrix, to the Operation or Division General Managers for all matters related to production and products.

Additionally, each product group has a Q & R organization under a single manager. This involvement on product specific levels provides the Customer and Intel with the timely response needed to maintain a product that meets all the customer expectations and totally complies with internal and external specifications. Should a problem arise, it is handled quickly and effectively at local levels, and elevated, if need be, to the rest of the organization. This results in a "team" approach among quality, reliability, design engineering, manufacturing, procurement—making state-of-the-art technology available in usable form to our customers.

## COMPONENTS QUALITY AND RELIABILITY ORGANIZATION

Consistent with the Corporate Quality Policy and Culture, the Components Quality and Reliability Organization has the following charter:

To insure that Intel's component products and services meet all our customers' expectations. To be the catalyst for providing the education, training, motivation, and tools needed for continual quality improvement throughout Intel.

The principle directions being taken to meet that charter are:

- Assure continually improving reliability of manufacturing technologies and processes.
- Design quality and testability into our products.
- Provide support to customers which meets all of their expectations.

The Component Quality and Reliability is organized to fully support these major thrusts.

## COMPONENT MANUFACTURING QUALITY AND RELIABILITY

The Manufacturing Quality and Reliability organization consists of five major groups who are responsible for the development, qualification, and continual improvement of the quality and reliability of Intel's processes and packages.

- 1. Process Reliability**—responsible for doing fundamental reliability studies on Intel's Fab processes and defining the design and process parameters under which reliability of the products can be assured.

2. **Package Reliability**—responsible for doing fundamental reliability studies on Intel’s assembly processes. Additionally, this group qualifies and monitors all assembly processes, assembly plants and package types.
3. **Production Plant Quality and Reliability**—groups reside in each plant and are responsible to assure that quality and reliability goals consistent with customer needs are met.
4. **Reliability Monitor System**—responsible for defining and maintaining a reliability monitor system which provides the data which demonstrates that quality and reliability expectations are being met.
5. **Materials Quality Control**—responsible for ensuring that all piece parts and raw materials meet Intel’s needs for the production of reliable quality components. MQC engineers develop inspection procedures for masks, chemicals, gasses, and package components and work with our vendors to help them solve their quality problems.

## PRODUCT QUALITY AND RELIABILITY

The product Quality and Reliability organizations are responsible for assuring that all Intel components meet our requirements and customers’ expectations for quality and reliability. To achieve this goal design methodologies are established to assure all process design rules and testability goals are met during the design process. In addition, product qualification methods are established to assure that products meet reliability goals. Finally, manufacturing check points are established to assure that all product shipped meets customers’ expectations.

## CUSTOMER QUALITY AND RELIABILITY

The Customer Quality and Reliability organization is responsible to understand and communicate our customers’ expectations and to define actions which assure that they are met. To achieve these goals, Customer Quality and Reliability has created regional customer quality support centers which provide direct customer interface to communicate and resolve customer issues and problems. Customer Quality Reliability also assures that an appropriate quality system exists throughout the company to meet these goals.

## COMPONENT QUALITY PROGRAMS

### Component Qualification

The key to establishing a new product, process or package, or to changing an existing one, is meeting the rigid qualification requirements. Qualification must be run and approved by the appropriate reliability department before any revenue shipment can be made. The reliability goals which have been set during the concept stage must be demonstrated by the qualification. Consider one example, the qualification of a new wafer fab technology for one time programmable EPROMs. The first five wafer lots face the following tests during qualification:

125°C burn-in	168 hours
125°C lifetest	2000 hours
150°C HTRB	1000 hours
Low-temperature lifetest	1000 hours
250°C storage	1000 hours
85°C/85% RH	1000 hours
Steam	168 hours
Temperature cycle	– 55°C to + 125°C
Thermal shock	– 55°C to + 125°C
Test pattern study	
Program/erase cycling	
System verification	

The sequence of tests determines infant mortality, random failure rates, and associated failure mechanisms. This data also becomes the basis of reliability reports made available to our customers.

## Component Reliability Monitoring

While successful completion of qualification is the key to product introduction, it would be meaningless if the device were not sampled throughout its product life. On a rotating product bases, 125°C dynamic burn-in and lifetests are performed continuously to monitor all technologies. Fifty thousand devices each month are allocated for the Reliability Monitor Program by the Components Division. In this manner, all generic technology families are continuously scrutinized to ensure that reliability goals are met.

In the same manner, Intel Package Reliability performs an extensive package monitor program to ensure the mechanical integrity of every package type produced by every assembly facility.

## FA/CR's (Failure Analysis/Correlation Request)

The need for an Intel-customer correlation effort has grown with device complexity. In response to this need, an FACR (Failure Analysis Correlation Request) system has been established within each division or operation. Operating through the Field Sales Engineers, the object of the program is to eliminate electrical test discrepancies between Intel and its customers in a timely manner. The system provides direct contact with a product-oriented Quality Engineer to eliminate test program or equipment discrepancies between the customer and Intel without returning all products shipped. The success of the program may be measured by the number of lots that have been shipped to customers and have been questioned and accepted after utilizing FACR system. The obvious by-product of this system is to build customer confidence to the point where Intel's final test and FQA data becomes the customer's incoming inspection data.

## Military

The Military Quality Assurance program, operated out of the Phoenix site, attends to customers within the aerospace or military industry or in some cases, to customers who have special documentation requirements. To perform in this product area, the Military Q.A. acts as an overlay on all sites and operations, defining the Q.A. program requirements in that particular area. The success of this program may be gauged by the acceptance of selected high-technology products by the Federal Government, and the product processing areas certified by an agency of the Federal Government. This department also performs process audits on a regular basis of applicable Intel manufacturing facilities to ensure compliance to rigid military traceability and process requirements.



# SYSTEMS GROUP QUALITY AND RELIABILITY (SQR)

## ORGANIZATION

The Systems Group SQR organization is comprised of a central policy and standards group and a matrixed manufacturing site process and product audit group. SQR activities are in accordance with current internationally recognized standards for quality programs. Specifically, SQR is organized to support ANZI 1.8 and Z 1.15 standards. SQR is an integral part of all phases of a product's life cycle. SQR audits internal practices and organizations to assure control and foster continuous quality improvement.

### 1. Systems Group Reliability Engineering (SGRE)

Administers the reliability program, develops new methods for predicting and demonstrating product reliability, and performs fundamental product reliability research. SGRE also manages the Systems Group environmental lab which standardizes product evaluations for vibration and shock, temperature and humidity, and reliability demonstration testing.

### 2. Systems Materials Quality Engineering (SMQE)

Manages the overall quality program for procured items as a member of Intel's Materials Commodity Management Team. Performs supplier selection, survey, and qualification activities. Monitors supplier's process and Intel's factory yield of commodities to focus on continuous quality improvement. Certifies suppliers who demonstrate process control to enter our dock-to-stock preferred vendor program.

### 3. Customer Quality Team (CQT)

Provides liaison with customers for all quality related matters. Produces monthly management reports with indicators of product performance in the field based on customer inputs. Champions the resolution of quality problems by responsible Intel organizations to assure the customer's problem does not recur.

### 4. Manufacturing Site QA (SQA)

Responsible for process and product audits performed to monitor production quality and focus corrective actions to assure continuous quality improvement. SQA is matrixed to the Director of SQR to assure uniform technical standards and policies.

### 5. Strategic Programs and Technologies

Provides long-term quality improvement programs which integrate quality technologies and processes into design, manufacturing, and administrative operations. Key programs such as statistical process control (SPC) are organized, trained, and implemented. Integrated quality information management computer programs and data analysis techniques are developed and implemented.

### 6. Corporate Components Engineering (CCE)

Responsible for the selection, qualification, and control of all commercial electronic parts used in the designs of systems products. Provides component engineering analysis of components and Intel applications to ensure their proper specification in designs. CEE is matrixed to the Director of SQR to assure uniform technical standards and policies and reports administratively to Design Engineering.

### 7. Product Safety Engineering (PSE)

Responsible for the evaluation and acceptance of all designs for product risk analysis, for regulatory agency compliance (such as UL, CSA, UDE, IEC, FCC), and management of field product safety programs.

### 8. Systems Group Peripherals Organization (SGPO)

Responsible for development of high-performance, cost effective I/O processors and selects and qualifies mass storage peripheral devices used in Intel Systems products. SGPO engineers are chartered in controller development, device qualification, evaluation, application engineering and supplier relationships.



## PRODUCT QUALITY

Controlling product quality and reliability is a complex task requiring a high degree of integration, organizational involvement and use of specialized disciplines, notably:

- Design Control through part selection and application, design rules, circuit analysis, derating requirements and assiduous environmental and reliability qualification testing. Key to this task is that reliability engineering is part of the product development team, and thus influences the design from the onset.
- Procured Material Control through a rigorous supplier selection, qualification and monitoring process. Our computerized supplier control system automatically assures procurement only from selected, qualified and approved sources. The privilege for any supplier to be on our approved list must be earned, while being included in our "Dock-to-Stock" program provides significant benefits to the suppliers as well as to Intel.
- Product Quality Monitoring and control through our automated reporting and analysis systems. Our system provides the right information to the Quality & Manufacturing engineers for early adverse trend detection. It also allows for product and process improvement through a corrective action system. But the final measure of our outgoing product quality is our continuous product sampling program, where finished product is subjected to a "customer audit". Only products which meet the stipulated quality levels may ship.
- Customer Quality Team reporting system completes the cycle. This full system provides timely feedback and gives us the ability to rapidly improve the product design and manufacturing processes.

Our approach to quality is based on a very fundamental policy: **DO IT RIGHT THE FIRST TIME**, while our quality philosophy is structured on two Intel corporate objectives. **OUR PRODUCTS MUST MEET THE CUSTOMERS NEEDS AND BE IN ABSOLUTE COMPLIANCE TO OUR SPECIFICATIONS.**

To provide you with additional insight on how the Intel Systems Group operates and assures quality of all products and services, a video tape presentation is available entitled "INTEL SYSTEMS—SUCCESS BY DESIGN". Other sources of information, more product and process specific, are our Systems Quality/Reliability Handbook and our Reliability Reports, of which a number have been released. All of these can be obtained from your Distributor or Intel Salesperson.

## MICROPROCESSORS

The Intel 86 Architectural Family starts with the standard 8/16-Bit 8088/80C88, and the highly integrated 80188 microprocessors. Our 16-bit microprocessor line consists of the industry standard 8086/80C86, the cost-effective, highly integrated 80186 and the powerful 80286 microprocessor with advanced multi-tasking and memory management capabilities. Our newest addition, the 80386 32-bit high performance CHMOS microprocessor offers such capabilities as demand paging, on-chip MMU and multi-tasking support.

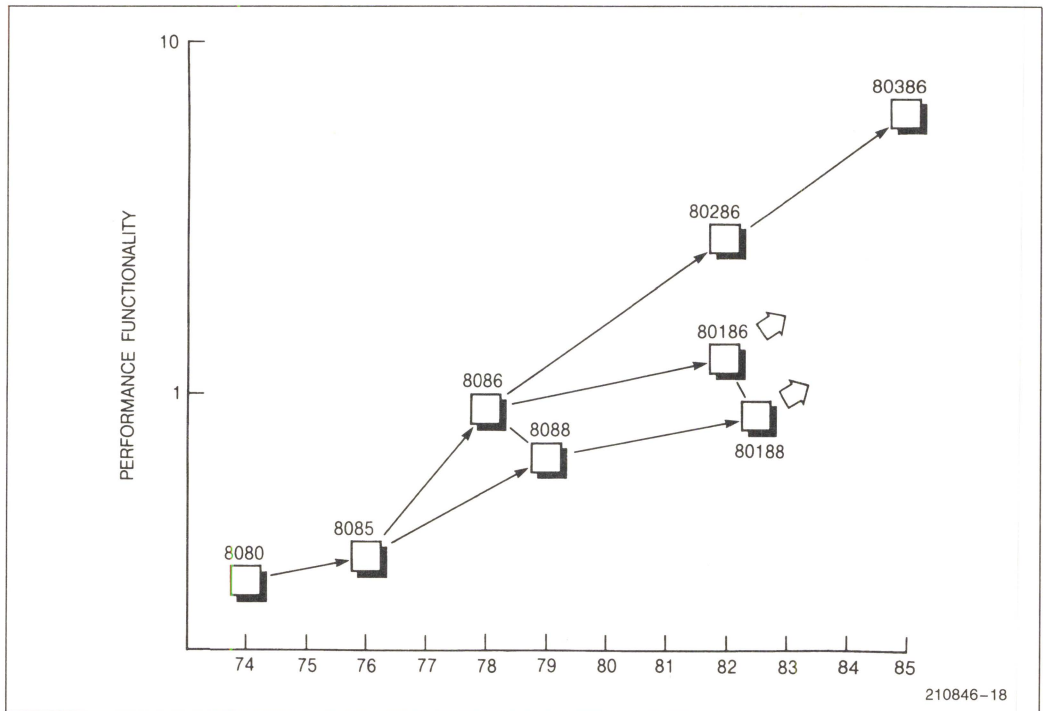


Figure 1. Microprocessor Families

### 8080/8085 8-BIT MICROPROCESSORS: Please reference Embedded Controllers

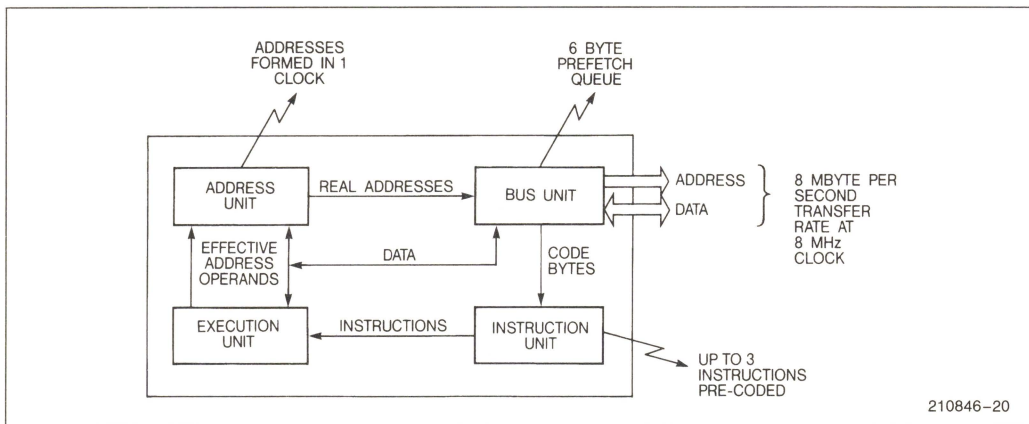
### 8086/8088 (CHMOS and HMOS)

The 8086/8088 includes the 8086/80C86 (16-bit bus) and the 8088/80C88 (8-bit bus) CPUs plus a complete set of supporting devices. Because the 8086 and the 8088 share the same 16-bit internal architecture, they are completely software-compatible and can use the same support components. This allows complete and full migration of software from 8- to 16-bit, and 16- to 8-bit systems. The 8086/8088 have achieved industry standard status with a 6-year track record of production and availability and numerous second sources. This family is fully compatible with Intel's complete line of coprocessors, a unique set of VLSI devices that allow system level architecture and performance customization. The 8086/8088 is also available in low-power CHMOS type.

### 80186/80188: Please reference Embedded Controllers

## 80286

The 80286 CPU is an advanced high performance 16-bit microprocessor with on-chip memory management and protection and hardware support for multiuser, multitasking systems. The pipelined architecture of the 80286, an 8 Mb/sec bus and a 3.5  $\mu$ s interrupt response time, at a clock frequency of 8 MHz gives it six times the performance of a standard 5 MHz 8086. The on-chip memory management and protection scheme is flexible, sophisticated and easy to use. It supports virtual memory of up to 1000 M Bytes/user. The four-level protection model provides task/task and user/operating system protection. The 80286 is also upward compatible with 8086/8088 and has a numeric processor extension (80287) that is compatible with the 8087 and an advanced DMA controller, 82258 (ADMA) for I/O processing.



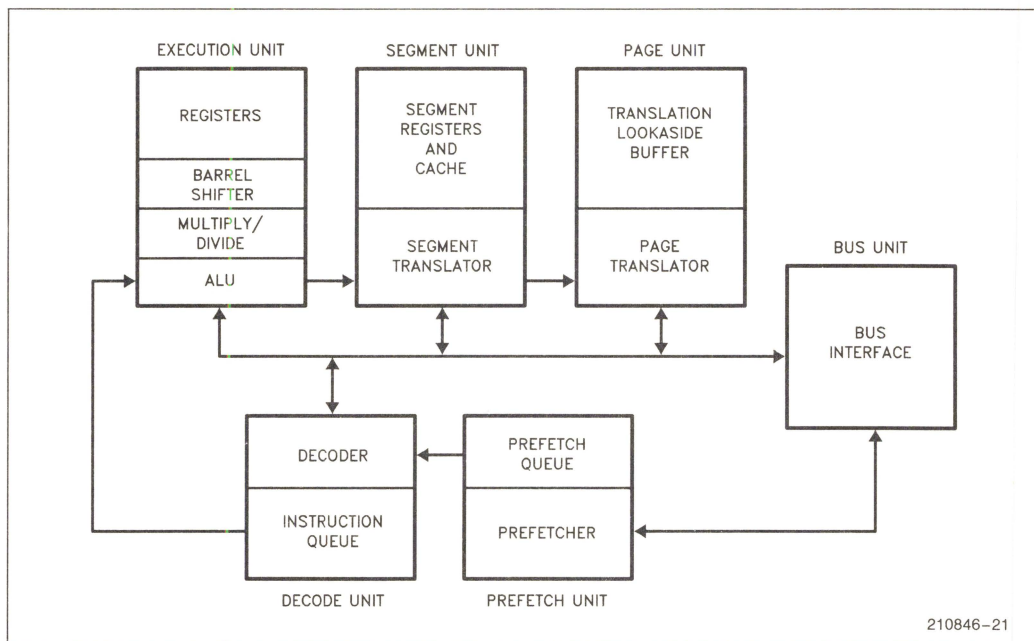
**Figure 2. 80286 Pipelined Microarchitecture**

The 80286 is binary compatible with the 8086/8088, 80186/80188 to allow simple migration of the large base of software for those machines to the 80286. The 80286 also has its own complete line of coprocessors for system architecture and performance optimization.

## 80386

The 80386 is an advanced 32-bit microprocessor designed for applications needing very high performance and optimized for multi-tasking operating systems. The 32-bit registers and data paths support 32-bit addresses and data types. The processor addresses up to four gigabytes of physical memory and 64 terabytes ( $2^{46}$ ) of virtual memory based on demand paging segmentation or both. The integrated memory management and protection architecture includes address translation registers, advanced multitasking hardware and a protection mechanism to support operating systems. In addition, the 80386 allows the simultaneous running of applications from multiple operating systems.

Instruction pipelining, on-chip address translation, and a high bus bandwidth ensure short average instruction execution times and high system throughput. The 80386 processor is capable of execution at sustained rates of between 4 and 6 million instructions per second.



**Figure 3. 80386 Pipelined Microarchitecture**

Object-code compatibility with all 8086 family members (8086, 8088, 80186, 80188, 80286) means the 80386 offers immediate access to the world's largest microprocessor software base. Of special interest is the 80386's unique virtual machine capabilities which allows direct execution of 8086 family software under new 32-bit operating systems.

The 80386 offers new testability and debugging features. Testability features include a self-test and direct access to the page translation cache. Four new breakpoint registers allow conditional or unconditional breakpoint traps on code execution or data accesses, for powerful debugging of even ROM-based systems.



Table 3. Microprocessors

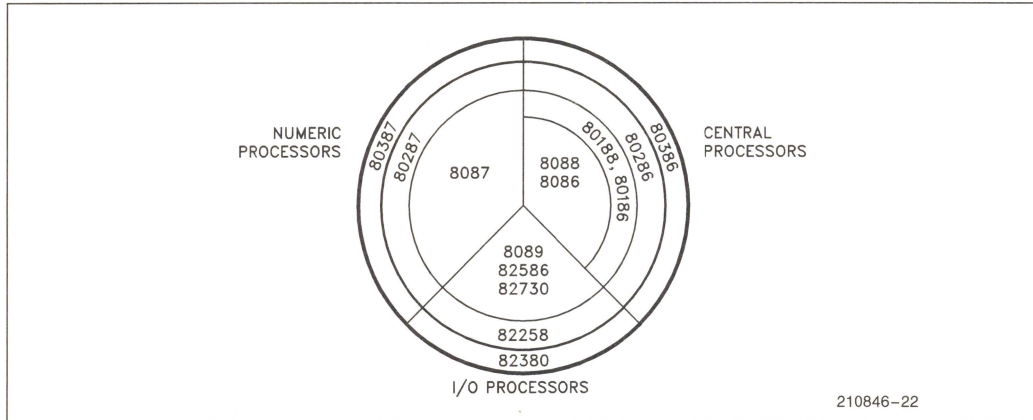
Features		Microprocessors							
		8080A (MCS-80)	8085AH (MCS-85)	8086/80C86	8088/80C88	80186	80188	80286	80386
<b>A. ARCHITECTURE</b>									
Bus Interface (Bits)		8	8	16	8	16	8	16	32
Internal Data Path (Bits)		8	8	16	16	16	16	16	32
Clock Frequency (Speed Selection)		2, 2.6, 3 MHz	3, 5, 6 MHz	5, 8, 10 MHz	5, 8 MHz	8, 10, 12.5 MHz	8, 10 MHz	6, 8, 10, 12.5 MHz	16, 20 MHz
Bus Band Width (Max)		0.75M bytes/s	1.5M bytes/s	5M bytes/s	2M bytes/s	6.25M bytes/s	3.12M bytes/s	12.5M bytes/s	32M bytes/s
Register to Register (Min) Add Time ( $\mu$ s/data word)		1.3 $\mu$ s	0.67 $\mu$ s	0.3 $\mu$ s	0.38 $\mu$ s	0.2 $\mu$ s	0.3 $\mu$ s	0.125 $\mu$ s	0.1 $\mu$ s/ dataword
Interrupt Response Time (min)		7.3 $\mu$ s	2 $\mu$ s	6.1 $\mu$ s	8.6 $\mu$ s	3.36 $\mu$ s	6.2 $\mu$ s	2.5 $\mu$ s	3.5 $\mu$ s
Memory Addressability		64 KB	64 KB	1 MB	1 MB	1 MB	1 MB	16 MB	4 Gigabyte
Virtual Memory		No	No	No	No	No	No	Yes 1G byte/task	Yes 64 Terabyte/task
On-Chip Memory Management and Protection		No	No	No	No	No	No	Yes	Yes w/demand paging
I/O Addressability		256 Bytes	256 Bytes	64 KB	64 KB	64 KB	64 KB	64 KB	64 KB
Addressing Modes		5	5	24	24	24	24	24	28
Coprocesor Interface		No	No	Yes	Yes	Yes	Yes	Yes	Yes
No. of Registers	Arithmetic	1	1	8	8	8	8	8	8
	Index	1	1	4	4	4	4	4	8
	Segment	0	0	4	4	4	4	4	6
	General Purpose	6	6	8	8	8	8	8	8
Code Compatibility		8080A Code		8086 Code		8086 Code		8086/80286	

Table 3. Microprocessors (Continued)

Features		Microprocessors							
		8080A (MCS-80)	8085AH (MCS-85)	8086/80C86	8088/80C88	80186	80188	80286	80386
B. SOFTWARE SUPPORT									
High Level Languages	A wide variety of third party software products are available, see Software Section for Intel products.								
Operating Systems									
C. DEVELOPMENT SUPPORT: See Development Tools and Software Section									
D. KEY PERIPHERAL SUPPORT CHIPS: See Peripherals Section, Page 27.									
Clock Generator	8224	On-Chip	8284A	8284A	On-Chip	On-Chip	82284	82384	
System Controller	8228/38	On-Chip	8288	8288	On-Chip	On-Chip	82288	TTL or PAL	
Interrupt Controller	8259A	8259A	8259A	8259A	On-Chip	On-Chip	8259A	8259A/82380	
DMA Controller	8257	8237A	82258	8237/ 82258	On-Chip/ 82258	On-Chip 82258	82258	82258/82380	
Timer-Counters	8253	8253/8254	8253/8254	8253/8254	On-Chip	On-Chip	8253/8254	8253/8254/82380	
Data Bus Transceiver	8216/8226	8286/8287	8286/8287	8286/8287	On-Chip	On-Chip	8286/8287	8286/8287	
DRAM/Controller	8203/82C03	8203/82C03	8207/8208	8207/8208	8207/8208	8207/8208	8207/8208	PAL	
Chip Select/Wait State Logic	TTL	TTL	TTL	TTL	On-Chip	On-Chip	TTL	TTL or PAL	
Math Processor			8087	8087	8087	8087	80287	80287 or 80387	
E. GENERAL									
Package	Pins	40	40	40	40	68	68	68	132
	Type	DIP (P&D)	DIP (P&D)	DIP (P&D)	DIP (P&D)	LCC (Leadless) PLCC (Leaded) PGA	LCC (Leadless) PLCC (Leaded) PGA	LCC (Leadless) PLCC (Leaded) PGA	PGA
Power Supply		± 5V, 12V	5V	5V	5V	5V	5V	5V	5V
Military/Express	See Military and Express Sections								

## COPROCESSING—A NEW ARCHITECTURAL CONCEPT

The 8086 family brought with it a new architectural concept called “coprocessing”. Basically, the task to be handled is partitioned into functional areas such as central processing, I/O processing and numerics support. For each functional area there is a device that extends the CPU’s register and instruction sets. In this way, the cost of the specialized hardware is incurred only when required, and the chip-set is optimized for specific applications.



**Figure 4. Processing—Function Partitioning**

For numeric intensive applications, the 8087, 80287 and 80387 numeric coprocessors extend the base architecture by adding 8 eighty-bit registers and about 70 instructions. By executing floating point routines in hardware, performance is improved up to 100X. Eighty-bit precision maximizes accuracy while conforming to the proposed IEEE standard for floating point execution.

I/O intensive applications are supported by the 82258 (ADMA). This device enhances system performance by taking I/O load off the CPU. The 82258 is a 16-bit, high speed (8M Byte/sec transfer rate in 8 MHz 80286 systems) DMA as processor with on-chip bus interface for the whole 8086 architecture (8086/88, 80186/188, 80286, 80386). Four independently programmable channels, including a multiplex or channel supporting 32 subchannels, can handle a large number of I/O devices.

The 82586 LAN Coprocessor is an I/O coprocessor that concurrently processes the ISO open system interconnect model levels 1 and 2 for local area networks with various topologies, framing techniques, contention detection schemes and carrier methods.

The 82730 Text Coprocessor is an I/O coprocessor that concurrently processes text manipulation tasks. It interprets pointer table linked list data structures, allowing high resolution text displays to modified “instantaneously” without loading the microprocessor. Display formats are very flexible, allowing system designers to program displays to satisfy their unique requirements.

**Table 4. Numeric Processors**

Device Number	Function	Description	CPU	Speed	Package Type/ No. of Pins
8087	Numeric Processing	Performs arithmetic, logical and transcendental operations on 32-, 64-, 80-bit floating point operands, 32- and 64-bit integers and 18-digit BCD operands to greatly enhance speed of system. Floating point operations are approximately 100x faster than equivalent CPU/software routines. Accuracy is extended to 80 bits. Meets proposed IEEE standard (#754).	8086/8088 80186/ 80188	With 5 MHz clock 14/18 $\mu$ s 32 Bit Multiply: 19 $\mu$ s 64 Bit Multiply: 27 $\mu$ s Divide 39 $\mu$ s With 8 MHz clock 32 Bit Multiply: 11.9 $\mu$ s 64 Bit Multiply: 16.9 $\mu$ s	Ceramic 40
80287	Numeric Processing	Performs arithmetic, logical and transcendental operations on 32-, 64-, 80-bit floating point operands, 32- and 64-bit integers and 18-digit BCD operands to greatly enhance speed of system. Floating point operations are approximately 100x faster than equivalent CPU/software routines. Accuracy is extended to 80 bits. Meets proposed IEEE standard (#754). Has an asynchronous interface to the 80286 which allows the 80286 and 80287 to operate at different speeds in a system.	80286 80386	With 5 MHz clock 14/18 $\mu$ s 32 Bit Multiply: 19 $\mu$ s 64 Bit Multiply: 27 $\mu$ s Divide 39 $\mu$ s With 8 MHz clock 32 Bit Multiply: 11.9 $\mu$ s 64 Bit Multiply: 16.9 $\mu$ s	Ceramic 40
80387	Numeric Processing	Supports all operations of the 80287 plus additional functions such as simultaneous sine and cosine. Overall performance is 4 to 6 times 80287's (5 MHz).	80386	16 MHz and 20 MHz	68 Pin PGA



**Table 5. I/O Processors**

Device Number	Function	Description	CPU	Speed	Package Type/ No. of Pins
82586	Local Area Network Coprocessor	Implements Ethernet and IEEE 802.3 specifications, manages transmission/reception processes w/o CPU intervention including command and data buffer chaining network management and diagnostic functions.	8085AH 8086/8088 80186/80188	8 MHz	CC/48
82730	Text Coprocessor	Provides high quality text display, proportional spacing, superscript/subscript, etc. High performance text manipulation-onboard DMA, high-level commands and table driven linked list data structure. Programmable bus interface—8 or 16 bit data and 16 or 32 bit addressing. Flexible display formats programmable at screen and row level. Simultaneous display of independent data bases.	ALL	8 MHz-Bus 10 MHz-Character	C/68
82258	Advanced DMA Processor	16 bit, 4 channel DMA controller with on-chip bus interface for the whole 8086 architecture (8086/8088, 80186/80188, 80286 and 80386). Provides high speed DMA transfers.  Increases system performance because of its I/O processing capabilities through command and data chaining. Large number of medium to slow speed devices can be handled by the multiplex or channel supporting 32 subchannels. Data manipulation is done through "On the Fly" compare, translate and assembly/disassembly operations. Remote mode of operation allows modular designs.	8086/88 80186/188 80286 80386	8M Byte/sec in 8 MHz 80286 systems 4 MByte/sec in 8 MHz 8086/80186 systems. 16 MByte/sec in 80386 systems	LCC/68 PGA

## DEVELOPMENT TOOLS

Intel recognizes that developing a product based on an advanced microprocessor creates major challenges for an engineering group. Intel helps you meet these challenges and keep your project under control with a set of development tools tailored to the architecture you are using. These tools help you get your product development done within your schedule and budget targets by solving problems that waste valuable engineering time.

The first key to productive product development is to work on your product instead of developing and integrating tools. Intel has tools for each phase of your project, and each of them works smoothly with the others to form an effective, integrated tool set. The tools work on popular industry-standard systems, including the IBM PC AT\* and PC XT\* and compatible personal computers and Digital Equipment Corporation VAX/VMS\* Systems.

\*VAX/VMS are trademarks of Digital Equipment Corporation. IBM, PC XT, and PC AT are trademarks of International Business Machines Corporation.

### HIGH-LEVEL LANGUAGE SUPPORT

Each Intel microprocessor and microcontroller is supported by a set of high-level languages that have the three important elements of well-integrated tools:

The most important integration is between the tools and the processor. Intel assemblers and compilers are optimized around the architectures they support: that means better performance for your product. And efficient compilers mean you can write more of your code in high-level languages instead of assembly language.

Effective coding generally requires a family of compatible translators so that you can draw on the most appropriate language to implement each part of a design. PL/M, Pascal, C, FORTRAN, and assembly language enjoy certain advantages over each other, depending on the application. You can link object modules from any of the Intel translators without further modifications.

The symbolic debugging power of Intel's debuggers is enhanced by communication between the translators and debuggers.

**Table 6. Development Languages and Utilities**

Product	Description
Assemblers	All Intel assemblers—and there's one for every major Intel component—provide full macro support.
PL/M	PL/M was the first high-level language designed expressly for microprocessors. It is a procedure-oriented language with data structuring facilities that gives the engineer full control over microprocessor-dependent architecture features. It is one of the most widely used tools in the microprocessor and microcontroller world.
C	C-86 is a true implementation of the C programming language defined by Keringhan and Ritchie. C is known for its flexibility and portability.
Pascal	Pascal-86 and Pascal-286 are supersets of ISO Pascal, with extensions for independent compilation and port I/O. They also embody advanced code optimization techniques to achieve extremely efficient programs.
FORTRAN	FORTRAN-86 and FORTRAN-286 are ANSI-77-standard compilers augmented with full 8087/80287 support and the ability to handle very large arrays (over 64 KB).
Utilities	Intel linkage utilities allow independent assembly and compilation of program modules. Library managers allow the management of standard modules and routines. In the case of 80286, a system builder is provided to allow easy configuration of a complex protected/ memory-managed system.

## HARDWARE AND SOFTWARE DEBUGGERS

Intel has made debuggers a part of each microprocessor family package, beginning with ICET<sup>™</sup> 80, the world's original in-circuit emulator. Intel's debuggers have the power to find bugs early, while they are still cheap and easy to fix, and to find many bugs that would not otherwise be fixed without a major waste of engineering time and schedule time.

Intel's popular In-Circuit Emulators (ICET<sup>™</sup>) continue their key role in development projects, with full-speed, transparent debugging for Intel components. Intel ICE debuggers feature symbolic debugging, the ability to stop execution under user-determined conditions, trace collection, and emulation memory for program execution.

### DEBUGGERS FOR 8086 AND 80286 FAMILY MICROPROCESSOR APPLICATIONS AND 80186 EMBEDDED CONTROLLER APPLICATIONS

Intel's debugging product line for the 8086, 80186, and 80286 families of microprocessors features a pair of powerful tools covering the full range of development needs:

Debugging Task	Tool
Host-resident, high-level software debugging	PSCOPE
Full-speed, transparent software hardware integration and debug	I <sup>2</sup> ICET <sup>™</sup> Emulator

The tools share a common user interface and high-level language debugging capability. Symbolic debugging automates a task that can eat up valuable development time and introduce error into the debug process. Symbolic debugging builds on the debug records loaded from the output of Intel assemblers and compilers—yet another example of the added debugging power gained from integration of development tools. Using user-defined names, the engineer has access to memory locations and program variables (including dynamic variables and high-level-language data structures).

#### PSCOPE High-Level Language Debugger

PSCOPE is a host-resident debugger that lets you execute and debug programs at the source code level. You can set break and trace points, examine memory, or simply follow program flow at the instruction, statement or procedure level for programs written in PL/M, Pascal, C, FORTRAN, 8086 assembly language, or 80286 assembly language. PSCOPE even lets you make high-level language patches and store them for later use in updating source files.

The PSCOPE syntax, including debug procedures, is the same used by the I<sup>2</sup>ICET<sup>™</sup> and TargetSCOPE systems, so when you move from software development to software-hardware integration, the user interface stays the same. There's no new learning curve to ascend, no lag in the development cycle.

#### I<sup>2</sup>ICET<sup>™</sup> Integrated Instrumentation and In-Circuit Emulation System

I<sup>2</sup>ICE is unmatched in its ability to kill hardware and software bugs across the entire development process. Of course, I<sup>2</sup>ICE offers the high-level language symbolic debugging expected of a software debugger. It also integrates transparent emulation support for all members of Intel's 8086 and 80286 families of microprocessors.

A full I2ICE configuration can simultaneously emulate four separate processors, stopping execution on an individual event, on an address range, on conditional events and on inter-processor events. The system then displays a trace of execution or bus activity. Full-speed execution is possible using either target system memory or up to 288 K-bytes of emulator memory for each processor.

## PERFORMANCE ANALYSIS

The iPAT Performance Analysis Tool provides real-time performance analysis and real-time test coverage of programs running on 8086/88, 80186/88, and 80286 microprocessors to help software engineers optimize code and improve software reliability.

Object code generated by Intel assemblers and compilers (C, PL/M, Pascal, and FORTRAN) can be analyzed symbolically to improve software efficiency and to validate test coverage. Any object code that lacks compiler information—but that can be run by Intel emulators and for which an absolute program map is available—can also be analyzed non-symbolically by the iPAT analyst.

## DEBUGGERS FOR 80386 FAMILY MICROPROCESSOR APPLICATIONS

Users of Intel's 80386 advanced, 32-bit microprocessor have a compatible set of software and hardware debugging tools available for their projects:

Debugging Task	Tool
High-level software debugging	PSCOPE Monitor 386 (P-MON 386)
Software debugging monitor	Debug Monitor 386 (D-MON 386)
Full-speed, transparent software hardware integration and debug	ICE 386 Emulator

### PSCOPE Monitor (P-MON 386)

P-MON 386 is a high-level, hosted software debugger for 80386-based systems. It can access and control all of the 80386's visible user hardware resources without any resistance from the operating system. It can also be used to debug applications running under the control of an operating system.

P-MON 386 allows symbolic debugging of programs written in high-level languages. With the help of this debugger, a user can download an application program into the target prototype memory, set hardware and software breakpoints at symbolically specified addresses, trace program execution, and write patches to the program under development.

### Debug Monitor 386 (D-MON 386)

D-MON 386 is an unhosted, EPROM-based software debug monitor that provides system-level debug support for 80386 systems. Using D-MON 386, a user can set hardware and software breakpoints, examine and modify memory and registers, and control program execution. This monitor can be configured to run on any 80386-based target board with a user-supplied communication driver and hardware initialization routine.



## **ICE™ 386 In-Circuit Emulator**

The ICE 386 In-Circuit Emulator provides hardware and software debugging for 80386-based designs. Its capabilities include emulation for the 80386 CPU and the 80287 and 80387 numeric processors. With ICE 386, programs can execute continuously at speeds up to 16 MHz or in a single-step mode. And it includes symbolic debugging to let users work in the context of their original programs.

Intel designed the 80386 and ICE 386 interactively to get the debugging power required of an advanced, 32-bit microprocessors, including non-intrusive access to internal processor activity. Breakpoints allow stopping emulation on specified instruction execution addresses or data addresses. Trace capability lets a user record program execution history prior to the break.

## **DEBUGGERS FOR MCS-51 AND MCS-96 EMBEDDED CONTROLLER APPLICATIONS**

Microcontroller applications are typically characterized by high performance requirements, a variety of asynchronous events, and a lot of on-chip activity. All of these characteristics add to the challenge of debugging your product. Each Intel microcontroller family has in-circuit debugging support to meet the challenges. The ICE and VLSiCE emulators share a user interface with I<sup>2</sup>ICE and PSCOPE, which saves learning time for projects with multiple processor types.

## **ICE™ 5100 In-Circuit Emulator**

The ICE 5100 emulator gives its user, real-time, non-obtrusive control over 8051-family system debugging at clock speeds up to 16 MHz. It includes the ability to view and modify system activity at a symbolic, high-level language level. ICE 5100/252 debugs HMOS and CHMOS versions of the 8051, the 8052, and the 80C52, including on-chip RAM and ROM. The ICE 5100/044 supports the 8044, including BITBUST™ systems.

## **VLSiCE™ 96 In-Circuit Emulator**

VLSiCE 96 provides real-time, non-obtrusive debugging support for the MCS-96 family of 16-bit microcontroller components. It features full symbolic debugging; 64 K-bytes of mappable ICE memory; dynamic execution and data trace, including internal RAM accesses; and a break/state machine which allows stopping emulation or enabling trace on user specified combinations of execution addresses, opcodes, data addresses and values, and selected PSW bits.

## **ISBE 96 8096 Emulator**

The ISBE 96 debugger permits basic execution and debug of programs written for the MCS-96 family of 16-bit microcontrollers, within the emulator or in the user's target system.

## **GENERAL TOOLS FOR ALL COMPONENT FAMILIES**

### **EPROM Programming Support**

Intel offers a full line of EPROM programmers for Intel devices. Through parallel development efforts, Intel is able to provide the earliest programming support for new Intel EPROMs, EEPROMs, KEPROMs and microcontrollers—with the fastest programming algorithms in the industry. The modular architecture of Intel EPROM programmers allows new support to be added with low-cost add-ons, as they become available.

## EPLD Development Tools

Intel's iPLDS Programmable Logic Development System makes it easy to use an Erasable Programmable Logic Device (ELPD) in your design. The iPLDS provides all the software, programming hardware, and documentation needed to convert random logic into a fully optimized, tested, and documented device.

## AEDIT Text Editor

AEDIT is a full-screen text editor that can be either menu- or command-driven. It offers the ability to switch easily between two files or to view two files simultaneously through windows. Text entry and editing are further simplified through the use of macros, which allow you to save command clusters for later use.

## DEVELOPMENT HOSTS

Intel's development tools are available on a selection of industry-standard host systems, giving users of Intel microprocessor and microcontrollers the ability to apply a combination of valuable elements in their development projects:

- design and debug tools built around the needs of the specific microprocessor or microcontroller.
- host systems optimized around installed equipment or the experience and needs of the development team:
  - VAX/VMS                      Centralized development and project control for large teams, on an industry standard system.
  - PC AT, PC XT (DOS) Versatile, standard, high-performance workstation
- continued use of Inteltec® Series II, III, and IV and Model 800 dedicated development systems.
- an open network to link tools across the various host environments.

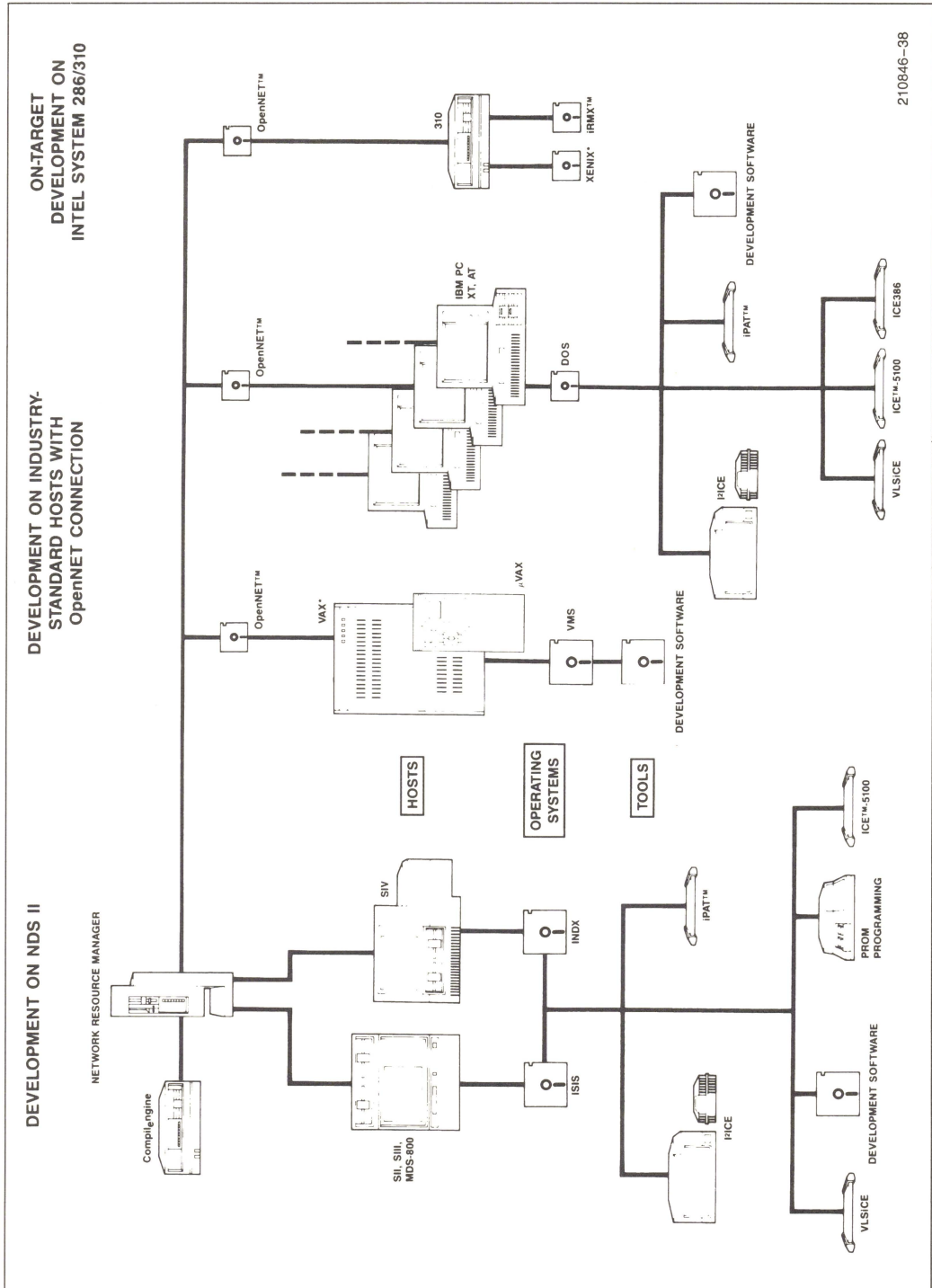
Whether you run the Intel tools on a VAX minicomputer, a PC AT or XT, or an Intel system, the integration work is done before you install the tools on the system—you don't waste time getting the tools ready for the project.

## NETWORK CONNECTIONS

Your host workstations can be a part of a complete development network using Intel's OpenNET™ implementation of the high-performance Ethernet local area network.

The OpenNET™ network is based on open, ISO OSI standard protocols. In a development application it lets your PC- and VAX-based development stations share files resident on the VAX system. The OpenNET connection also (1) lets PC users share files resident on Intel's NDS II Network Resource Manager and (2) gives users doing on-target development on Intel iRMX® and XENIX\* system access to files resident on a VAX/VMS, iRMX, XENIX, or DOS system from an iRMX, XENIX, or DOS system.

\*XENIX is a trademark of Microsoft Corporation.



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Figure 5. Tools Support on OpenNET™ Local Area Network

**Table 7. Component Support on Industry Standard Host Systems**

Components Supported					
	8086 80186 8088 80188	80286	80386	8096	8044 8051
<b>Development Languages</b>					
Assembler	PC VAX/VMS Series IV	PC VAX/VMS Series IV	PC VAX/VMS	PC Series IV	PC Series II Series IV
PL/M	PC VAX/VMS Series IV	PC VAX/VMS Series IV	PC VAX/VMS	PC Series IV	PC Series II Series IV
C	PC VAX/VMS Series IV	PC VAX/VMS Series IV	PC VAX/VMS	PC	
Pascal	PC VAX/VMS Series IV	PC VAX/VMS Series IV			
FORTRAN	PC VAX/VMS Series IV				
<b>Debuggers</b>					
PSCOPE	PC Series IV				
I <sup>2</sup> ICE™	PC Series IV	PC Series IV			
VLSiCE™				PC Series IV	
ICE™			PC		PC Series IV

**NOTES:**

Tools that run on Series IV or Series II also run on Series III.

Intel also offers versions of development languages that run on iRMX® and XENIX-based systems for on-target development.



## PERIPHERALS

Intel offers an extensive set of peripheral devices to augment microprocessor capabilities. The six major families of peripherals include: support peripherals, memory controllers, CRT display controllers, slave processors, math processors, and data communication controllers.

### MATH PROCESSORS

These devices process the data sent by the host CPU. Math and IEEE floating point calculations are implemented in hardware. This increases performance, reduces software overhead, and frees up the processor for other tasks.

**Table 8. Math Processors**

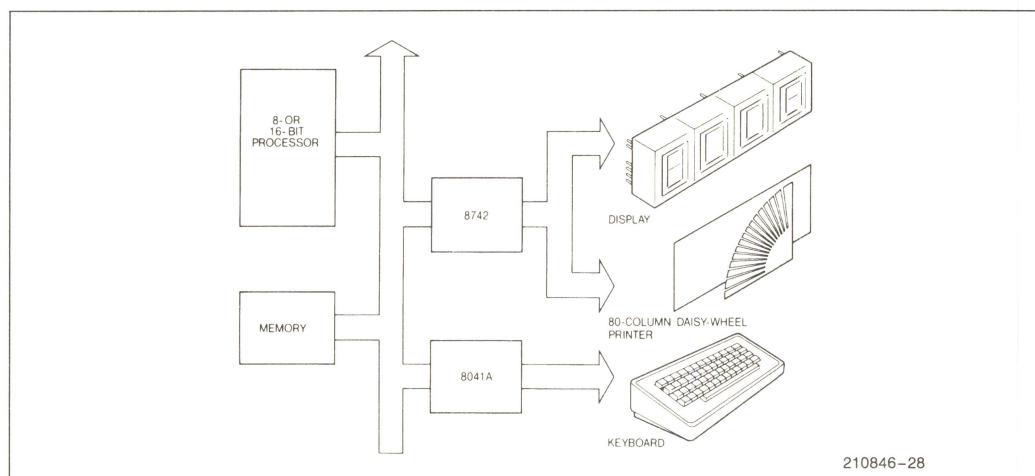
Device Number	Function	Description	CPU	Speed	Package Type/ No. of Pins
8087	Numeric Processing	Performs arithmetic, logical and transcendental operations on 32-, 64-, 80-bit floating point operands, 32- and 64-bit integers and 18-digit BCD operands to greatly enhance speed of system. Floating point operations are approximately 100 x faster than equivalent CPU/ software routines. Accuracy is extended to 80 bits. Meets proposed IEEE standard (#754).	8086/8088 80186/ 80188	With 5 MHz Clock 32 Bit Multiply: 19 $\mu$ s 64 Bit Multiply: 27 $\mu$ s Divide 39 $\mu$ s	CC/40
80287	Numeric Processing	Performs arithmetic, logical and transcendental operations on 32-, 64-, 80-bit floating point operands, 32- and 64-bit integers and 18-digit BCD operands to greatly enhance speed of system. Floating point operations are approximately 100 x faster than equivalent CPU/ software routines. Accuracy is extended to 80 bits. Meets proposed IEEE standard (#754). Has an asynchronous interface to the 80286 which allows the 80286 and 80287 to operate at different speeds in a system.	80286	With 5 MHz Clock 14/18 $\mu$ s 32 Bit Multiply: 19 $\mu$ s 64 Bit Multiply: 27 $\mu$ s Divide 39 $\mu$ s With 8 MHz Clock 32 Bit Multiply: 11.9 $\mu$ s 64 Bit Multiply: 16.9 $\mu$ s	LCC/40
8231A	Arithmetic Processing	16/32 Bit Integer and Floating Point Arithmetic	ALL	32 Bit Integer Multiply: 50 $\mu$ s 32 Bit Floating Point Sine: 1•1 $\mu$ s	C/40

## SLAVE PROCESSORS

Slave processors consist of a family of user programmable devices. They are “Universal Peripheral Interfaces” (UPI™), for control functions where no standard controller exists. These UPI devices are flexible single chip microcomputers with on-chip CPU, ROM or EPROM, RAM, I/O ports and a slave interface to the master system CPU. They allow the designer to integrate random control logic and to add custom control interfaces to a system.

UPI products include pin-compatible ROM and EPROM versions to allow prototyping/debugging or rapid feature upgrades in production. The instruction set is based upon the industry-standard 8048.

The UPI family is supported with a line of products for code development: development systems, assembler, in-circuit emulators (ICE) and PROM programmers.



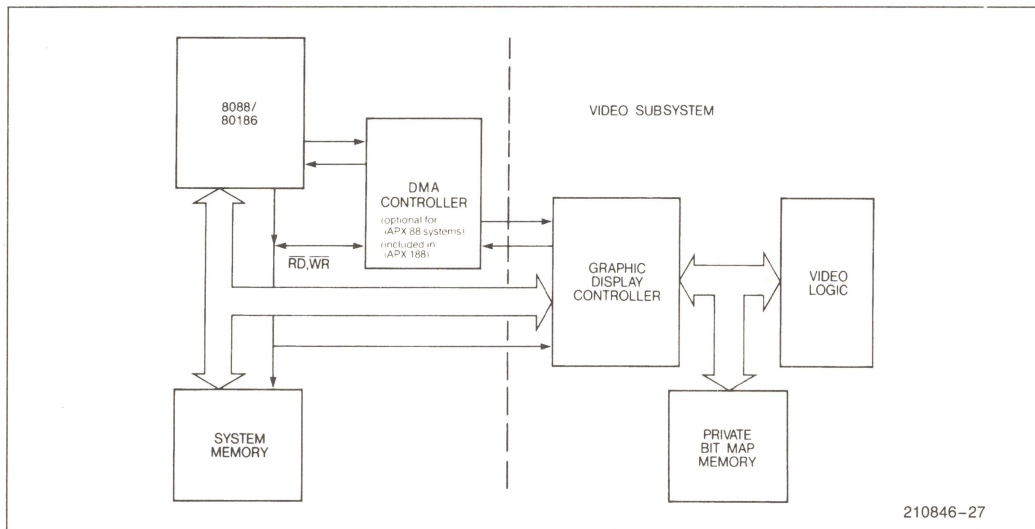
**Figure 6. Universal Peripheral Interfaces (UPI™) for Non-Standard Control**

**Table 9. Slave Processors**

Device Number	Function	Description	CPU	Speed	RAM	I/O Lines	Package Type/ No. of Pins
8041AH	UPI 1K ROM	Programmable Peripheral	8048	6 MHz	64 Bytes	18	P,D,N/40
8741AH	UPI 1K EPROM	Programmable Peripheral	8048	6 MHz	64 Bytes	18	D/40
8042AH	UPI 2K ROM	Programmable Peripheral	8049	12 MHz	286 Bytes	18	P,D,N/40 N/44
8742AH	UPI 2K EPROM	Programmable Peripheral	8049	12 MHz	256 Bytes	18	P,D/40 N/44
80C452	UPI ROMless	I/O Processor	8051	16 MHz	256 Bytes	40	A/68
83C452	UPI 8K ROM	I/O Processor	8051	16 MHz	256 Bytes	40	A/68
87C452	UPI 8K EPROM	I/O Processor	8051	16 MHz	256 Bytes	40	A/68
8243	I/O Expansion	UPI I/O Expander adds 16 lines to UPI controller	8041A 8042 8048 8049 8050	—	—	16	P,D/40

## CRT DISPLAY CONTROLLERS

Intel's CRT display controllers are designed to display information on a CRT screen with a wide variety of screen formats. They are also the only chips designed to reduce the display manipulation task for the system microprocessor, improving overall system quality and performance.



**Figure 7. CRT Display Controller Subsystem**

**Table 10. CRT Display Controllers**

Device Number	Function	Description	CPU	Screen Formats	Display Types	Speed Selections	Package Type/ No. of Pins
8275	Programmable CRT Controller	Programmable screen and character format, 6 independent field attributes, 11 visual character attributes, cursor control, light pen capability, programmable DMA mode.	MCS 80/85 8086/8088 80186/80188 MCS-51	80 char/row 64 rows/frame	Alpha-Numeric	2 MHz(Std) 3 MHz(- 2)	P,D/40
8276	Small System CRT Controller	Programmable screen and character format, 6 independent field attributes, cursor control, on-chip dual row buffers, cascadable up to 4 controllers.	MCS 80/85 8086/8088 80186/80188 MCS-51	80 char/row 64 rows/frame	Alpha-Numeric	2 MHz(Std) 3 MHz(- 2)	P,D/40
82720	Graphics Display Controller	Provides microcomputer system with bit map graphics capabilities. Refreshes screen from a bit map RAM. Accepts high level commands which causes GDC to draw graphics figures into bit map memory concurrently with CPU operations.	ALL	Up to one mega pixel resolution	Alpha-Numeric; Graphic; Vector; Arc; Rectangle; Slant	4 MHz(Std) 5 MHz(- 1)	CD/40

**Table 10. CRT Display Controllers (Continued)**

Device Number	Function	Description	CPU	Screen Formats	Display Types	Speed Selections	Package Type/ No. of Pins
82730	Text Coprocessor	Provides high quality text and bit-map graphics display, proportional spacing, superscript/subscript, etc. High performance text manipulation-on-board DMA, high-level commands and table driven linked list data structure. Programmable bus interface—8 or 16 bit data and 16 or 32 bit addressing. Flexible display formats programmable at screen and row level. Simultaneous display of independent data bases.	ALL	Up to 200 chars/row 2048 scan lines/frame	Alpha-Numeric Alpha-mosaic, mixed text and graphics with 82720	Separate system and video clocks, maximize overall system performance	CP/68
82731	Video Interface Controller	Parallel to serial data conversion on-chip dot clock generator, dot rates up to 50 MHz 16 dot wide character. Proportional spacing and attribute generation support. Works with the 82730 text coprocessor.	—	—	—	50 MHz dot rate	P,D/40
82716	Video Storage Display Device	Highly integrated, low cost display controller. Implements graphics displays with a minimum of chips. On-chip DRAM control, CRT control, video line buffers, color palette, and D/A converters. Flexible object structures support animation and windows. Can sync to external video sources for overlay.	ALL	640 x 512 pixels mono or Color	Graphics and character	20 MHz dot rate	CGA/68 PLCC/68
82786	Graphics Coprocessor	Provides high performance graphics and high quality text with advanced display control. Full support for graphics primitives at up to 2.5 million pixels per second and bit-mapped proportionally spaced text up to 25 thousand characters per second. Hardware windows, zoom, cursor, pan and scroll. Separate graphics/text and display content control units. Integral DMA and DRAM controllers. Low power CHMOS. Linked list instructions.	ALL	Up to 3.6 mega pixel resolution	Mixed text & graphics; Display selected from output by multiple applications within many windows; to 256 colors.	10 MHz system clock; 25 MHz video clock	CG/68

## MEMORY CONTROLLERS

The memory controller family of peripherals integrates the logic required to interface dynamic RAM, floppy disks and Winchester disks to microprocessors.

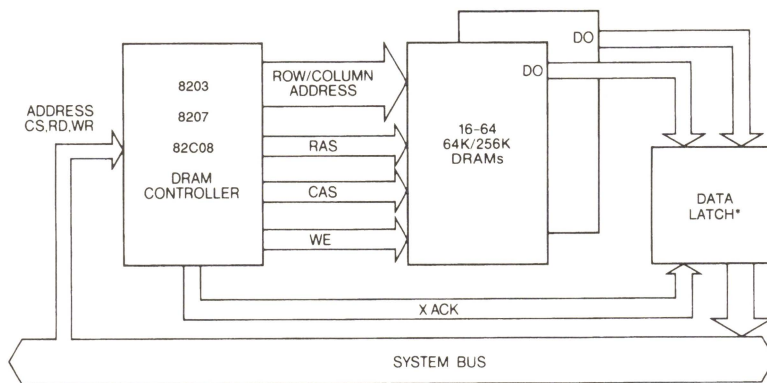
The dynamic RAM controllers supply all three functions necessary in any dynamic RAM design: row/column address multiplexing, refresh and arbitration. A single device replaces 10-15 TTL packs and the delay line. The 8207 extends the level of integration to include support for a dual-port interface, bank interleaving and complete ECC control with the 8206. The 82C08 is a single-chip low-power solution for DRAM control. It is ideal for low-power and portable systems.

Three other memory controllers interface a microprocessor to mass storage devices. The 8272A and 82072 control 3½", 5¼" and 8" disk drives, while the 82064 controls Winchester disk drives using the ST506 standard interface.



**Table 11. Memory Controllers**

Device Number	Function	Description	CPU	Speed	Memory Size	Package Type/ No. of Pins
8203	16K/64K DRAM Controller	Provides all logic to interface 64K DRAMs to any microprocessor	ALL	0–3 Wait states	256K Bytes	D/40
8206	Error Detection and Correction	Single-bit Correction Double-bit Detection	ALL	55 ns	8 bit to 80 bit words	A/R/68
8207	64K/256K DRAM Controller	Interfaces 64K/256K DRAMs while providing a dual-port interface bank interleaving and ECC control	ALL	0 Wait states up to 16 MHz	2 MBytes	A/R/68
82C08	64K/256K CMOS DRAM Controller	Interfaces 64/256K DRAMs (including 256K x 4) to high performance 8-bit and 16-bit Microprocessors. Has power-down feature which keeps memory alive using battery backup. Single chip solution saves boardspace	ALL	0 Wait states up to 20 MHz	1 MBytes	P/48 N/68
8272A	Floppy Disk Controller	Programmable Single or Double Density Controller for up to 4 drives	ALL	500 KB/s 300 KB/s 250 KB/s	3½", 5¼" or 8" Floppy	P,D/40
82072	Floppy Disk Controller	CHMOS Single-Chip Floppy Disk Controller	ALL	1 MB/s 500 KB/s 300 KB/s 250 KB/s	3½", 5¼" or 8" Floppy	P/40 N/44
82064	Winchester Disk Controller	CHMOS Winchester Disk Controller for ST506 Interface Drives	ALL	5 MB/s	5¼" or 8" Winchester Disk	P,D/40 N/44



\*Not necessary for 82C08

210846-26

**Figure 8. Dynamic RAM Subsystem**

## Interrupt Controllers

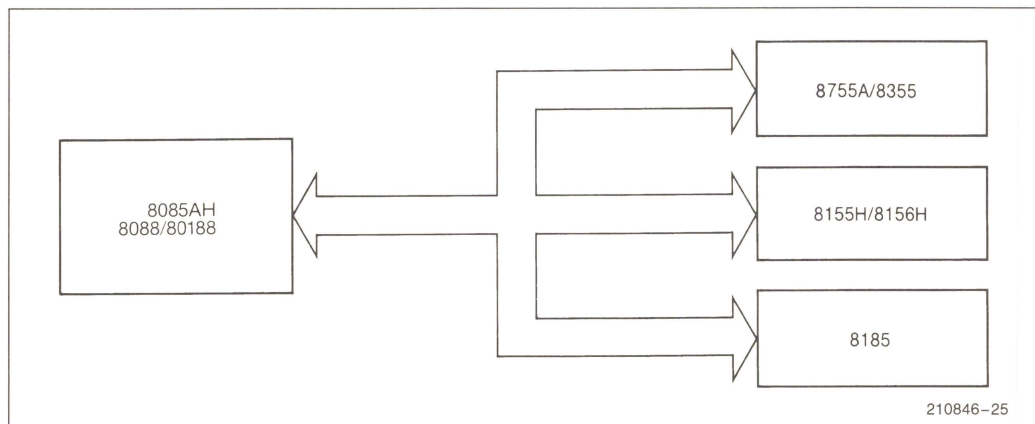
These provide faster response to real-time events in a large system without requiring the processor to poll for the source of peripheral service requests.

**Table 12. Interrupt Controllers**

Device Number	Function	Description	CPU	Package Type/ No. of Pins
8259A	Programmable Interrupt Controller	8 Vectored Interrupts, Cascadable to 64	ALL	P,D/28

## Multiplexed Memory Components

These Components can communicate over the multiplexed address/data bus of the MCS®-85, 8088 or 80188 processors eliminating the need for address latching.



**Figure 9. Multiplexed Memory Components**

**Table 13. Multiplexed Memory Components**

Device Number	Function	Description	CPU	Access Time	Package Type/ No. of Pins
8155H/ 8156H	Static RAM, I/O and Timer	256 bytes RAM; 14-bit counter/ timer, 22 parallel I/O-ports; internal address latch.	8085AH 8088 80188	330 ns (– 2) 400 ns (Std)	P,D/40
8185	Static RAM	1K X 8 RAM; internal address latch; low standby power requirements.	8085AH 8088 80188	250 ns (– 2) 350 (Std)	P,C/18
8355	ROM and I/O	2K X 8-bit Masked ROM; Two bidirectional 8-bit ports; internal address latch.	8085AH 8088 80188	300 ns (– 2) 450 ns(Std)	P,D/40
8755A	EPROM and I/O	2K X 8-bit Erasable PROM and I/O; Erasable with UV Light; Electrically reprogrammable; interchangeable with 8355.	8085AH 8088 80188	300 ns (– 2) 450 ns (Std)	DB/40

## Clock Generators and Bus Controllers

These devices include: clock generators, bus drivers, bus transceivers, bus controllers, bus arbiters and latches. They provide the drive, control signals and timing to directly support interfacing to the industry-standard MULTIBUS®.

**Table 14. Clock Generators and Bus Controllers**

Device Number	Function and Description	CPU	Package Type/ No. of Pins	Speed Selections
<b>For MCS-80/85 Controllers</b>				
8224	Clock Generator	8080A	P,D/16	3 MHz
8228/8238	System Controller and Bus Driver	8080A	P,D/28	3 MHz
<b>For 8086/8088 Processors</b>				
8282/8283	Octal Latch	8086 8088	P,D/20	—
8284A	Clock Generator and Driver	8086 8087 8088 8089	P,D/18	8 MHz 10 MHz
8286/8287	Bus Transceiver	8086 8088	P,D/20	—
8288	Bus Controller	8086/8088 80186/80188 8087 8089	D/20	8 MHz
8289	Bus Arbiter	8086/8088 80186/80188 8087 8089	P,D/20	8 MHz
<b>For 80286</b>				
82284	Clock Generator	80286	D/18	8 MHz
82288	Bus Controller	80286	D/20	8 MHz
82289	Bus Arbiter	80286 82258 (ADMA)	D/20	8 MHz
<b>For I/O Coprocessors</b>				
82285	Clock Generator	82586 82730	D/18	8 MHz

## SUPPORT PERIPHERALS

Intel's support peripherals are designed with a consistent bus interface that makes them compatible with the entire Intel microprocessor line, from 8 to 16 bits. As a result, the user can leverage previous design and learning investments with each microprocessor upgrade. This support includes the following products.

### Timer-Counters, Parallel I/O, Keyboard Controllers

These devices are used for baud rate generation, event counting, motor controls and real-time clock functions.

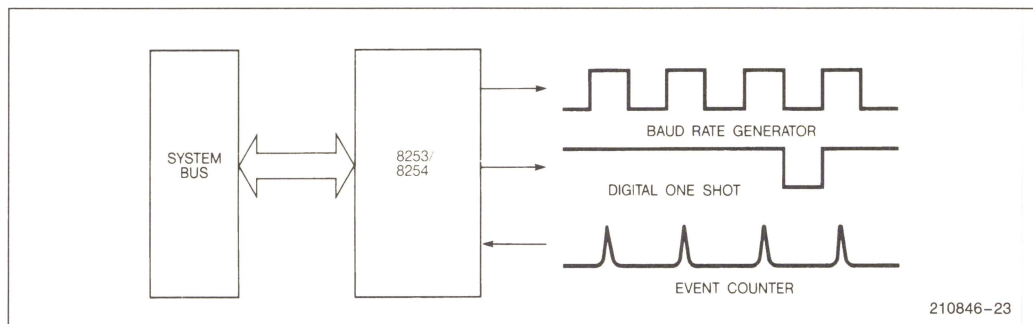


Figure 10. 8253/8254 Time/Counter

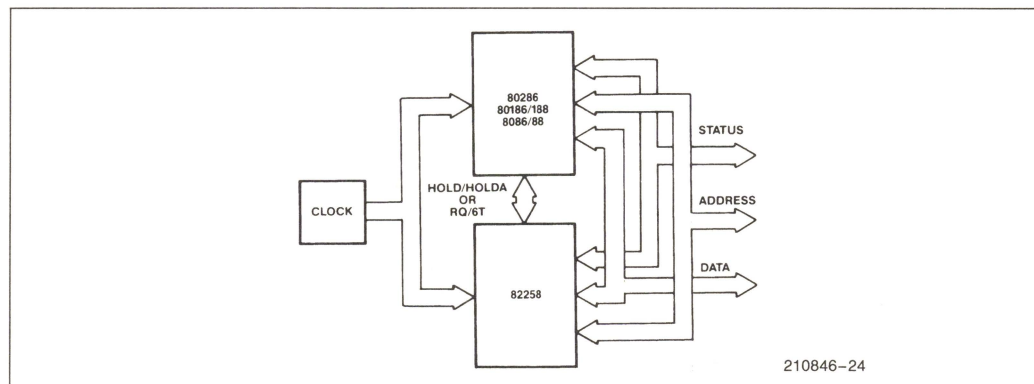
Table 15. Timer-Counters, Parallel I/O, Keyboard Controllers

Device Number	Function	Description	CPU	Speed	Package Type/ No. of Pins
8253	Timer/Counter	3 Independent 16-Bit Counters	ALL	2.6 MHz Count Rate	P,D/24
8254	Timer/Counter	3 16-Bit Counters—Superset of the 8253	ALL	10 MHz Count Rate	P,D/24
82C54	Timer/Counter	CHMOS, 3 16-Bit Counters Compatible with 8254	ALL	10 MHz Count Rate	P,D/24 N/28
8255A	Parallel I/O	24 TTL—Compatible I/O Lines	ALL	—	P,D/40
82C55A	Parallel I/O	CHMOS, 24 TTL Compatible I/O Lines	ALL	—	P,D/40 N/44
8256AH	All Basic Support Functions	Serial I/O + Parallel I/O + Timer/Counters + Interrupt Control (8251A + 8253 + 8255A + 8259A)	ALL	UART: 1 MB/s Counters: 0.5 MHz	P/40
8279	Keyboard Controller	64-key keyboard and display scan control	ALL	—	P,D/40



## DMA Controllers

These devices are designed to offload the CPU while speeding up data transfers in the system by allowing external devices to directly transfer data to or from system memory.



**Figure 11. 82258 in an Intel Advance Processor Architecture System**

**Table 16. DMA Controllers**

Device Number	Function	Description	CPU	Speed	Package Type/ No. of Pins
80287	Numeric Processing	Performs arithmetic, logical and transcendental operations on 32-, 64-, 80-bit floating point operands, 32- and 64-bit integers and 18-digit BCD operands to greatly enhance speed of system. Floating point operations are approximately 100x faster than equivalent CPU/software routines. Accuracy is extended to 80 bits. Meets proposed IEEE standard (# 754). Has an asynchronous interface to the 80286 which allows the 80286 and 80287 to operate at different speeds in a system.	80286	With 5 MHz clock 14/18 $\mu$ s 32 Bit Multiply: 19 $\mu$ s 64 Bit Multiply: 27 $\mu$ s Divide 39 $\mu$ s With 8 MHz clock 32 Bit Multiply: 11.9 $\mu$ s 64 Bit Multiply: 16.9 $\mu$ s	LCC/40
8089	2-channel intelligent I/O Processor with DMA	Two I/O channels offer flexible, intelligent DMA operations and I/O program execution. In "local mode," the 8089 is closely coupled with an 8088 or 8086 CPU to add DMA capabilities with minimum chip count. In "remote mode," the 8089 serves as an I/O subsystem to maximize performance and flexibility.	8086 8088 Local Mode ALL Remote Mode	1.25 Mbytes/sec (5 MHz)	D/40
8237A	High Performance DMA Controller	4 independent DMA channels, can be cascaded to support any number of channels, additional feature of memory-to-memory transfer.	ALL	1.6 Mbytes/sec	P,D/40
8257	DMA Controller	4 channel DMA controller.	8080A 8085AH	960 Kbytes/sec (3 MHz)	P,D/40

## MICROCOMMUNICATIONS COMPONENTS

### INTEL'S MICROCOMMUNICATIONS

Intel is dedicated to improving your company's performance and productivity with a broad spectrum of communication networking products ranging from our OpenNET Networking Product family including systems, boards, and networking software to communication components, modules and systems that provide a new range of versatile, low-cost alternatives for connecting micro- and minicomputers to mainframes.

Intel's experience and leadership in state-of-the-art VLSI technology is leading the way in providing innovative, flexible and reliable communications networking solutions for our customers. Only through continued advances in VLSI can you unlock the communication bottlenecks that exist in today's multivendor office and industrial environments.

Intel's Microcommunication—that is, VLSI-based digital communication products and services is providing the vital elements lacking among various networks employed throughout the world. Advances in VLSI have allowed Intel to design advance microprocessor architectures such as the 80286 and 80386. These microprocessors when combined with various communication products provide the high performance, flexibility, and reliability necessary to simplify and improve communications. Thus improving the decision-making processes and creating a new level of information accessibility for your organization.

### Intel's Microcommunications Product Solutions

Intel's broad spectrum of microcommunications solutions include:

- OpenNET™ Software & Module Product Family
- LAN Network Products, Board and Component Level
- FASTPATH for Mainframe Connectivity
- MultiSERVER™ File and other Network Services
- Telecommunication Modules, Components and Software
- BITBUS™ Microcontroller Interconnect
- Wide Area Network Communication Solution—UARTs, Modems and ISDN
- Automatic Test System Modules and Components

The remainder of this section discusses each of Intel's Microcommunication product offerings. For more in-depth technical information refer to the Microcommunication Handbook for data sheets, article reprints, application notes and other technical information.

### OpenNET™ Product Family

Intel's OpenNET product family includes a broad spectrum of Local Area Network building blocks including communications modules, OpenNET software products and LAN components. The OpenNET product family is available to support all seven layers of the Open Systems Interconnection (ISO) model.

### OpenNET™ Software

The OpenNET software products which include iRMX Networking Software, XENIX Networking Software and the iNA 960 Transport and Network Layer Software are based on industry standard networking protocols and provide transparent remote file access interoperation between XENIX, iRMX, VAX/VMS, and PC/DOS or MS/DOS systems.

OpenNET MAP-NET™ Communication Software, along with iNA 960 Transport and Network Layer Software, is available in configurable and pre-configured versions to provide an ISO-SOI layers 3–7 implementation of the MAP (IEEE 802.4) specification. This software executing on an Intel iSBC® 554 board provides a complete seven layer MAP solution.

Complete seven layer Ethernet solutions are available in various configurable and pre-configured versions for XENIX and iRMX environments as well. These include either of the iSBC or iSXM 552 Ethernet Communication Engines or the iSBC 186/51 Communications Computer in conjunction with the iNA 960 or iNA 961 Transport and Network Layer Software and the iRMX Networking Software (iRMX-NET) or XENIX Networking Software (iXNX-NET).

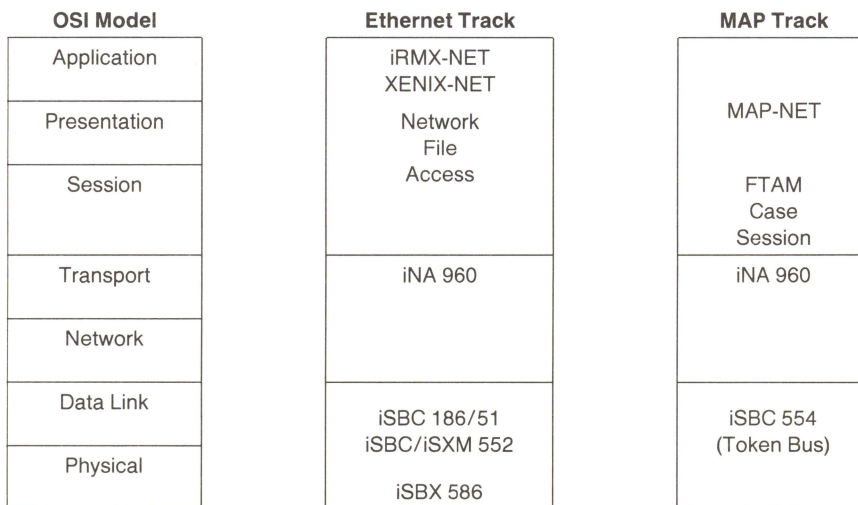
Intel's iNA 960 and its derivative iNA 961 implement the industry standard ISO 8073 transport protocols and ISO 8473 network protocols. These provide reliable end-to-end message delivery between two networked systems on an IEEE 802.3/Ethernet or an IEEE 802.4 Token Bus LAN. iNA 960/961 is fully supported by Intel's IEEE 802.3 and IEEE 802.4 LAN hardware modules.

The iRMX Networking Software (iRMX-NET) and XENIX Networking Software (iXNX-NET) products are based on the Network File Access protocols developed by IBM, Microsoft and Intel and provide transparent remote file access between XENIX, iRMX, VAX/VMS and PC or MS/DOS based systems. Transparent remote file access enables the user to work with remote files across the local area network as if they were local. iRMX-NET and XENIX-NET are supported by iNA 960/961 and Intel's LAN hardware modules. This set of products is intended to run in IEEE 802.3 environments.

The MAP Communications Software (MAP-NET™) includes FTAM, CASE, SESSION and Network Management/Directory Services and is intended to run in IEEE 802.4 environments.

Additional features and capabilities can be added to an OpenNET environment with the addition of Intel's Multi-SERVER™ and FASTPATH™ system enhancements. These are discussed in the Microcomputer Systems section of the product guide.

Furthermore, Intel's NDS-II (Network Development Systems) and OpenNET networks link tools hosted on Intel development systems with tools hosted on other industry-standard systems. This permits the host workstation to be an integral part of a complete development network using Intel's NDS-II and OpenNET/Ethernet networks, Intel's implementation of the high-performance IEEE 802.3 Ethernet Local Area Network. Additional information on Intel's NDS-II can be found in the Intel Development Systems Handbook.



**Figure 12. OpenNET™ Product Family**



## COMMUNICATIONS MODULES

### OpenNET™ Family of Local Area Network Products

Intel's LAN system building blocks are all part of the OpenNET product family. These modules allow the user to implement networks based on Ethernet (IEEE 802.3) and MAP (IEEE 802.4) that have transparent interoperability between multiple operating systems. The OpenNET modules listed in Table 17 cover layers 1 through 4 of the OSI reference model. Used together with Intel's iRMX and XENIX Networking Software or the MAP-NET™ Communications Software, the user can implement a complete seven layer solution for MULTIBUS systems. The OpenNET product line provides quick time-to-market networking solutions and LAN communications with IBM PCs and VAX/VMS systems.

**Table 17. OpenNET™ LAN Products**

Product	Description
iSBC 186/51 COMMputer™	<ul style="list-style-type: none"> <li>Integrates processing and communications capabilities onto a single board</li> <li>Ethernet (IEEE 802.3) and two serial (RS-232/RS-422/RS-449) connections supported</li> <li>Designed around the 80186 microprocessor and the 82586 LAN Coprocessors</li> <li>Two iSBX bus connectors for low cost expansion</li> </ul>
iSBC 552A IEEE 802.3 Ethernet COMMengine and iSXM 552A IEEE 802.3 Ethernet Transport Engine	<ul style="list-style-type: none"> <li>Dedicated Ethernet (IEEE 802.3) LAN Communications Engine</li> <li>Based on the 80186 microprocessor and the 82586 LAN Coprocessor</li> <li>Supports iNA 960 ISO Transport/Internetwork software</li> <li>Can be used with multiple operating systems</li> <li>iSXM 552A is preconfigured version providing a turnkey solution for ISO layers 1-4</li> </ul>
iSBC 186/530 MULTIBUS II IEEE 802.3/ Ethernet COMMengine	<ul style="list-style-type: none"> <li>Dedicated Ethernet (IEEE 802.3) LAN Communications Engine</li> <li>MULTIBUS II iPSB (Parallel System Bus) Interface with full message passing capability</li> <li>Based on the 80186 Embedded Controller and the 82586 LAN Coprocessor</li> <li>Supports iNA 960 ISO Transport/Internetwork Software</li> </ul>
iSBX 586 Ethernet Data Link Engine	<ul style="list-style-type: none"> <li>Low cost solution for Ethernet (IEEE 802.3) connections</li> <li>Single wide iSBX MULTIMODULE for use with MULTIBUS boards with 16-bit iSBX capabilities</li> <li>Takes advantage of the high performance 82586 LAN Coprocessor</li> <li>16KB of on-board buffer memory</li> </ul>
Intellink (DCM 911)	<ul style="list-style-type: none"> <li>Connects up to nine Ethernet compatible end nodes without the need for transceivers and coaxial cable</li> <li>Can be connected directly to an Ethernet cable through a standard transceiver and transceiver cable</li> </ul>
iSBC 554 MAP COMMengine	<ul style="list-style-type: none"> <li>Front End Communications Engine that supports a complete seven layer MAP solution</li> <li>10 Mbps IEEE 802.4 Broadband Token Bus Interface</li> <li>Supports Preconfigured iNA961 ISO Transport/Internetwork Software</li> <li>Intel's MAP Software for layers 5 through 7 can be run on-board</li> </ul>
iNA 960 Transport/Network Software	<ul style="list-style-type: none"> <li>Supports both Ethernet (IEEE 802.3) and MAP (IEEE 802.4) protocols</li> <li>Conforms to MAP 2.1 specification ISO Transport (8073) and Network (8473) standards</li> <li>Provides reliable "virtual circuit" process-to-process message delivery service</li> <li>Runs on 8086 and 80186 systems with the 82586 LAN Coprocessor</li> </ul>



## Point-To-Point Communications

Intel also provides the building blocks for point-to-point communications. These products can be used in terminal cluster control, modem control, host communications or general purpose applications. The product family supports a variety of communication electrical interfaces and protocols to allow open systems flexibility.

**Table 18. Point-to-Point Communication Modules**

Product	Description
iSBC 188/56 COMMputer™	<ul style="list-style-type: none"> <li>• Intelligent 8 channel single board system</li> <li>• 8 MHz 80188 and 256 Kbytes DRAM</li> <li>• Expandable to 12 channels via 2 iSBX 354</li> <li>• Supports ASYNC/SYNC, SDLC/HDLC</li> <li>• Supports RS232C on 6–8 channels, RS422 on up to 2 channels</li> </ul>
iSBC 88/45 ADCP (Advanced Data Communications Processor)	<ul style="list-style-type: none"> <li>• Intelligent communications controller can function as single board multimaster CPU or slave data comm gateway</li> <li>• 8 MHz 8088/10 (8088-2) Microprocessor</li> <li>• Three half/full duplex communication channels support HDLC/SDLC/ASYNCH/SYNCH operation</li> <li>• Two iSBX bus connectors to expand to 5 communication channels with iSBX 351 or iSBX 352 serial expansion MULTIMODULE boards</li> </ul>
iSBC 548 High Performance Terminal Controller	<ul style="list-style-type: none"> <li>• 8 RS232C Channels</li> <li>• 8 MHz 80186 and 128 Kbytes DRAM</li> <li>• On-board terminal handler firmware</li> <li>• Full RMX and XENIX Support</li> </ul>
iSBC 544 Intelligent Communications Controller	<ul style="list-style-type: none"> <li>• Acts as a single board communications controller or an intelligent slave for multi-terminal communications expansion</li> <li>• On-board dedicated 8085A CPU provides communications control and buffer management for 4 programmable synchronous/asynchronous channels</li> <li>• 10 programmable parallel I/O wires compatible with Bell 801 Automatic Calling Unit (ACU)</li> </ul>
iSBC 534 Four-Channel Communications Board	<ul style="list-style-type: none"> <li>• Four fully programmable synchronous and asynchronous serial communications channels</li> <li>• 16-bit parallel I/O interface compatible with the Bell 801 Automatic Calling Unit (ACU)</li> </ul>

**Table 19. MULTIBUS® Compatible iSBX™ Modules**

Product	Description
iSBX 586	<ul style="list-style-type: none"> <li>• IEEE 802.3/Ethernet Data Link Engine MULTIMODULE</li> </ul>

## LOCAL AREA NETWORK CONTROLLERS

Intel provides the broadest line of CSMA/CD devices available. High performance applications can utilize the 82586 LAN Coprocessor that supports IEEE 802.3 Ethernet and Cheapernet. Cost sensitive applications can use the 82588 Single Chip LAN Controller that supports emerging IEEE standards for PC networking: IBM PC Network and STARLAN. The 82586 is supported by iNA 960 Network software for quick time to market.

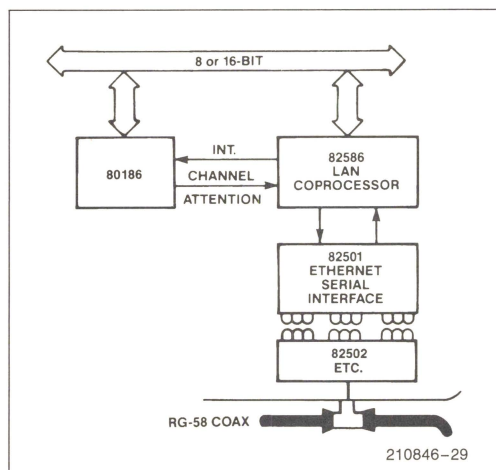


Figure 13. IEEE 802.3/Cheapernet Configuration

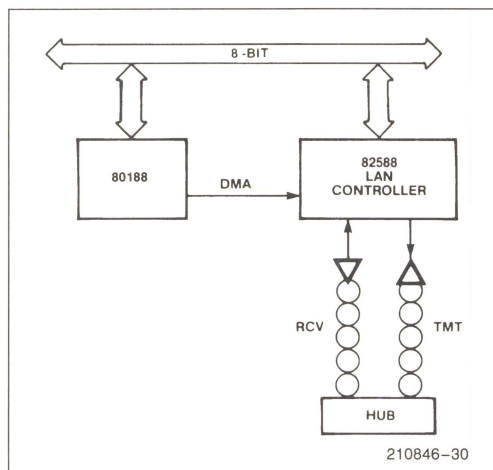


Figure 14. STARLAN Configuration

Table 20. Local Area Network Interface

Device Number	Function	Description	CPU	Encoding/Decoding	Protocols	Package Type/No. of Pins
82586	Local Area Network Coprocessor	Performs CSMA/CD Data Link Functions without CPU control. Performs memory management, and diagnostic on-chip. Programmable to be compatible with established and emerging IEEE standard. See iNA 960 Network Software.	8086 80186/ 80188	N/A	IEEE 802.3 Ethernet Cheapernet IBM PC Network STARLAN	CC/48
82588	Single Chip LAN Controller	High Integration Device that performs CSMA/CD data link control, encoding/decoding to 2 Mbps, and logic based collision detection in a single chip. Ideal for low cost LAN applications.	8086/8088 80186/ 80188	NRZI Manchester (1-2 Mbps)	IBM PC Network STARLAN	D/28
82C501	Ethernet Serial Interface	10 Mbps CMOS Manchester encoder/decoder. Drives and receives signals over 50 meter transceiver cable. Loopback capability for diagnostics. Used with 82586.	N/A	Manchester (10 Mbps)	IEEE 802.3 Ethernet Cheapernet	D/20
82502	Ethernet Transceiver	10 Mbps CMOS transceiver drives IEEE 802.3 standard 10 BASE 5 and 10 BASE 2 cable segments. Receivers from same. Provides watchdog timer function.	N/A	N/A	IEEE 802.3 Ethernet Cheapernet	D/16

## SERIAL DATA COMMUNICATION CONTROLLERS

The serial communication devices support all the serial standard protocols; asynchronous, byte synchronous and bit synchronous protocols. The interconnection can be local or remote. For remote channels, modem control lines are provided.

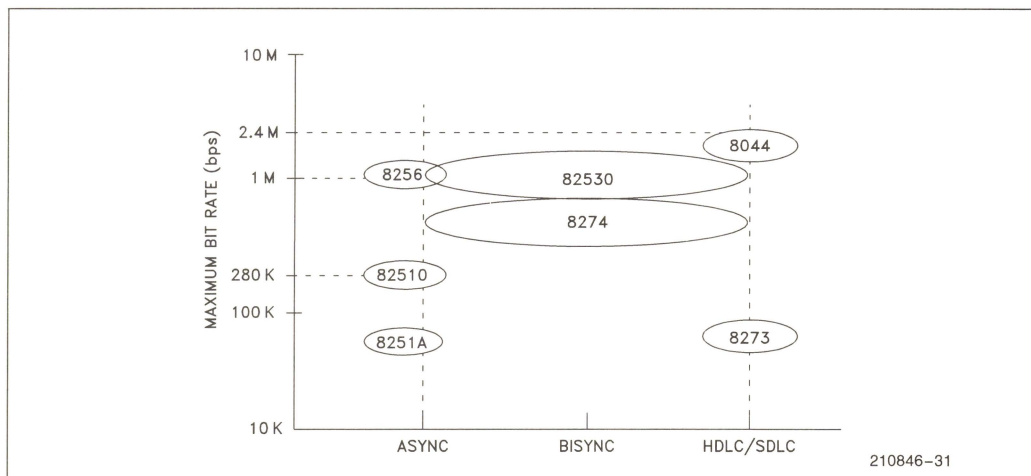


Figure 15. Data Comm Family

Table 21. Serial Data Communication Controllers

Device Number	Function	Description	CPU	Modem Control Lines	Serial Channel	ASYN	BISYNC	HDLC/SDLC	Max Data Rate	Package Type/No. of Pins
8251A	USART	Industry standard synchronous and asynchronous full duplex transmitter/receiver. Programmable priority bit, sampling rates, break generation and detection.	8080A 8085AH 8086/8088 80186/80188 8048AH/49AH 8051/8096	4	1	X	X	—	19.2K bps (Async) 64K bps (Bisync)	D/P/28
82510	High Integration CMOS UART	Single channel UART providing PC and PC plug-in compatibility. Provides 2-baud rate generators, supports 9-Bit Microlan protocol (8051 9-bit protocol), 4-byte FIFOs and control character detection. Applications also include terminals, serial backplanes, auto modem control. Runs PC software.	8085AH 8086/8088 80186/80188 8048AH/49AH 80286 80386 8051/8096	7	1	X	—	—	288 KB	D/28 PLCC
8256AH	Multifunction UART (MUART)	Full duplex asynchronous receiver/transmitter. Programmable baud rate generator. 16 parallel I/O lines. 8 level interrupt controller.	ALL	1	1	X	—	—	1M bps	P/40
8273	SDLC/HDLC Communications Controller	Interfaces $\mu$ P to SDLC/HDLC communication lines. Implements first level driver software in hardware. On-chip DPLL. Loop mode support.	8085AH 8086/8088 80186/80188 8048AH/49AH 8051/8096	3	1	—	—	X	64K bps	D/P/40
8274	Multiprotocol Serial Controller (MPSC)	Multiprotocol device with several $\mu$ P interface options. 4 independent DMA channels on-chip.	8085AH 8086/8088 80186/80188 8045AH/49AH 8051/8096	4 per channel	2	X	X	X	580K bps	D/P/40
82530	Serial Communications Controller (SCC)	Dual channel multiprotocol controller with on-chip baud rate generators, digital phase locked loops, various data encoding/decoding schemes and extensive diagnostic capabilities.	8085AH 8086/8088 80186/80188 8048AH/49AH 8051/8096 80286	4 per channel	2	X	X	X	1.5M bps	D/P/40
8344	High Performance 8-Bit Microcontroller with On-Chip Serial Communication Processor	8051 microcontroller core with high performance serial communication controller that can automatically respond to SDLC primary station commands. On-chip DPLL supports loop and non-loop.	—	2	1	—	—	X	2.4M bps	P/40
8044	—	8344 with 4K bytes of on-chip ROM.	—	2	1	—	—	X	2.4M bps	P/40
8744	—	8344 with 4K bytes of on-chip EPROM.	—	2	1	—	—	X	2.4M bps	C/40



## GENERAL PURPOSE INTERFACE BUS (GPIB) CHIP SET

### Introduction

The GPIB (General Purpose Interface Bus) has been with us now for eleven years. In 1975, the IEEE released the 488 Standard that defines an interface for programmable instruments. Since that time, the GPIB has been designed into hundreds of instruments in both the US and overseas. The interface is also being used for devices other than programmable instruments. Desktop computers and calculators use the GPIB to communicate with peripherals such as plotters, floppy disks, etc. In short, the GPIB enjoys wide acceptance and usage.

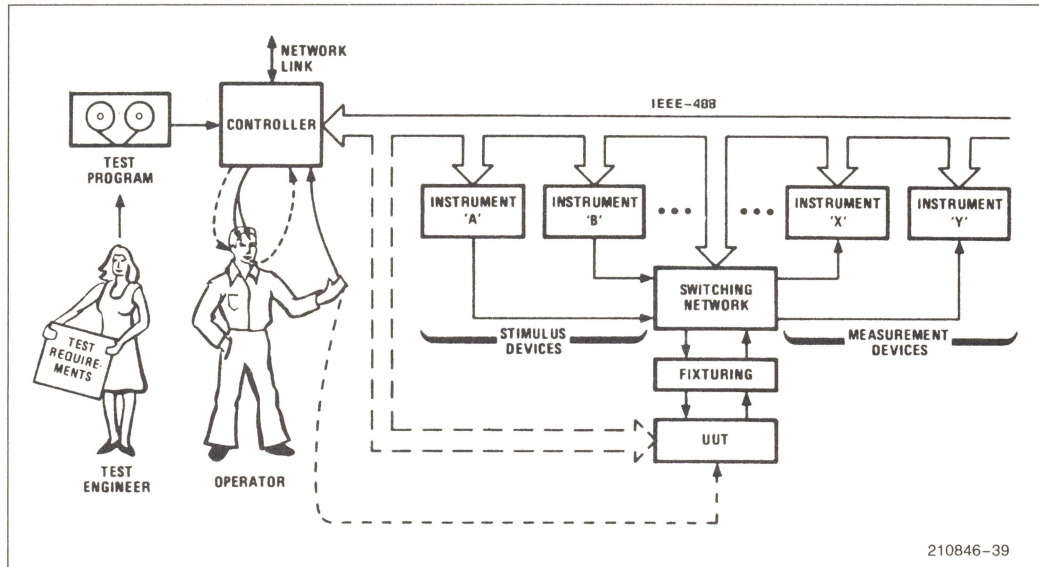


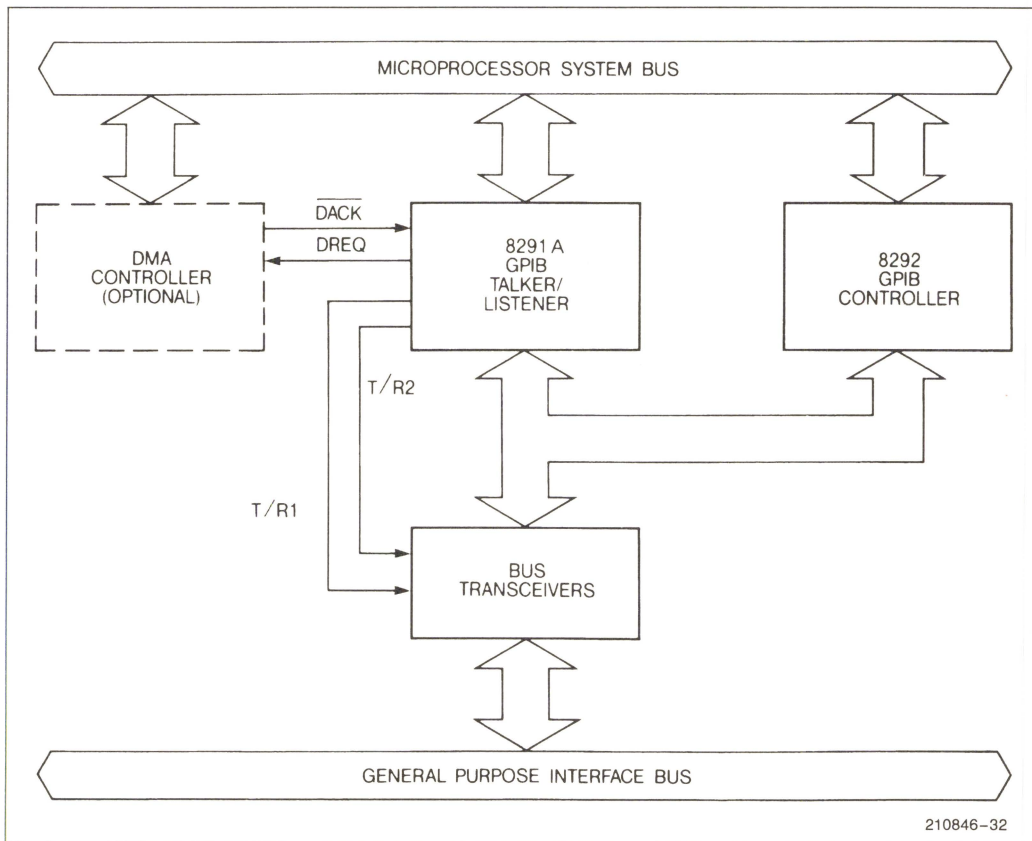
Figure 16. General Form of an Instrument System

## GPIB Products

The 8292 implements the Controller function of the IEEE Std 488-1978 (GPIB, HP-IB, IEC Bus, etc.). In order to function the 8292 must be used with the 8291 Talker/Listener and suitable interface and transceiver logic. In this configuration the system has the potential to be a complete GPIB Controller when driven by the appropriate software.

## GPIB Controllers

The 8291A/8292 are all the building blocks needed to implement the different types of nodes used on the GPIB (IEEE-488) parallel instrumentation bus.



**Figure 17. GPIB Controllers**

**Table 22. GPIB Controllers**

Device Number	Function	Description	CPU	Data Rate	Package Type/ No. of Pins
8291A	GPIB Talker/Listener	Complete talker/listener device that adheres to IEEE-488 standard. Implements all 9 talker/listener functions, on-chip programmable end of sequence register for automatic end of message.	8085AH 8086/8088 80186/80188 8048AH/8049AH 8051/8096	350K bps max	P,D/40
8292	GPIB Controller	Connects with the 8291A to form a complete IEEE-488 standard interface talker/listener/controller. Built in bus lock-up timers for high system reliability.	8085AH 8086/8088 80186/80188 8048AH/8049AH 8051/8096	N/A	P/40

**Table 23. GPIB Modules**

	Function	Description	iSBC	Data Rate	DC Power
iSBX 488	GPIB MULTIMODULE™ Board	<ul style="list-style-type: none"> <li>Provides talker/listener/controller functionality from any Intel iSBC board equipped with an iSBX connector to over 600 instruments and computer peripherals using IEEE-488 interface.</li> <li>Meets IEEE-488-1978 Standard.</li> <li>Software functions built into VLSI hardware for high performance, low cost and small size.</li> <li>Complete IEEE 488 controller functions including: transfer control, service requests and remote enable.</li> </ul>	All with iSBX Connector	350 Kbs	$V_{CC}$ + 5 VDC ± 5% $I_{CC}$ = 600 mA

## TELECOMMUNICATIONS PRODUCTS

The Intel Telecommunication product line consists of three generations of Telecom voice/data conversion products; the first generation Codecs and Filter; the second generation Combo Family; and the third generation of Advanced Telecom Components (iATC) for Integrated Services Digital Network (ISDN) applications.

In addition, Intel makes available a 2400 bps full duplex modem, providing a complete system solution in two chips.

The following lists all available Telecom component products:

### First Generation

- 2910A Industry Standard  $\mu$ -Law Codec
- 2911A Industry Standard A-Law Codec
- 2912A Industry Standard Filter

### Second Generation

- 2916/17 — 16 Pin  $\mu$ /A-Law Combo

### Third Generation

- 29C48 — Terminal SLD Combo
- 29C50 — MED Feature Programmable Combo
- 29C51 — High Feature Programmable Combo
- 2952 — Line Card Controller
- 29C53 — Four Wire ISDN Transceiver
- LEK 29C53 — Line Card Evaluation Kit
- TEK 29C53 — Terminal Evaluation Kit
- Modem-89024 — 2400 bps, FDX Modem Chip Set

## Codecs/Filter/Combos

Intel's PCM Codecs, Line Filters and Combo Chips are special purpose A/D and D/A converters and filters for use in PCM Line Circuits in telephony switching and transmission systems. The wide dynamic range (78 dB) and minimal conversion time (80  $\mu$ sec) also make them ideal for such other applications as voice store and forward, digital echo cancellers, secure communications systems, and satellite earth stations.

The 2910A/11A PCM Codecs and 2912A PCM Line Filter are industry standard components which have been in production for over eight years. We have shipped more than 25,000,000 Codec Filter or combo sets to date.

The new industry standard telephony line circuits are the 2913 and 2914 Codec/Filter Combo Chips. These devices have a fully differential internal architecture to improve crosstalk, idle channel noise, and power supply rejection. In addition, the transmit and receive channels are totally separate to further reduce crosstalk, and to improve performance in asynchronous operation. The charge-redistribution DAC has essentially eliminated gain tracking error. This superior transmission performance is combined with surprisingly low power dissipation through the use of our advanced HMOS-E technology; a proven technology which has supported the production of millions of 2764 EPROMs. For applications requiring especially low power levels (e.g., telephone handsets), CMOS combo chips are available.



**Table 24. Performance Comparison**

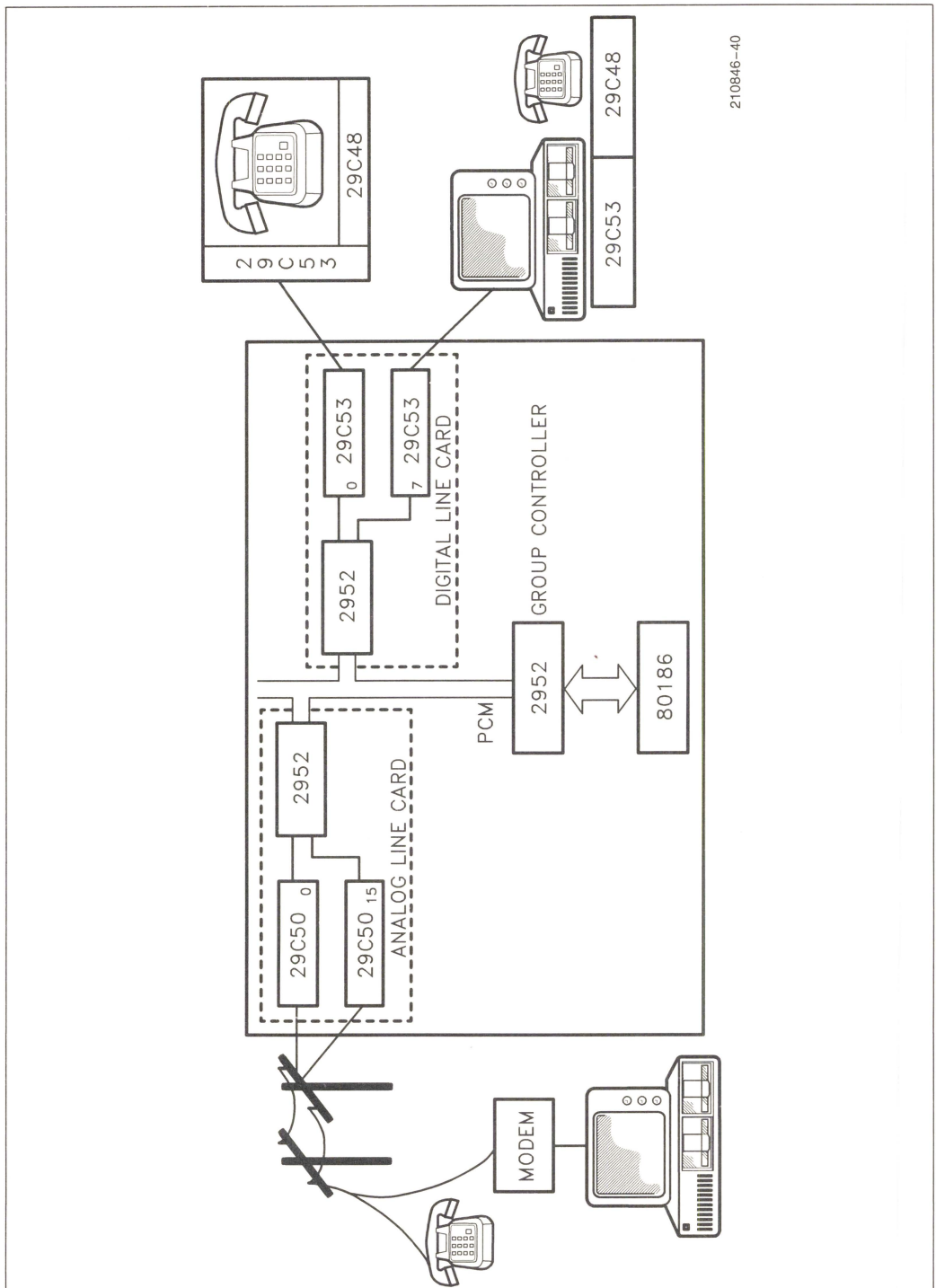
Features	2913 Codec/Filter Combo Chip	2914 Codec/Filter Combo Chip	2910A PCM Codec $\mu$ -Law	2911A PCM Codec A-Law	2912A PCM Line Filter	2916/17 Codec/Filter Combo Chip
Fixed Data Rate Mode	1.536, 1.544, 2.048 MHz	1.536, 1.544, 2.048 MHz	1.536, 1.544, 2.048 MHz	1.536, 1.544, 2.048 MHz	Compatible	2.048 MHz
Variable Data Rate Mode	64 kHz to 2.048 MHz	64 kHz to 2.048 MHz	No	No	Compatible	64 KHz to 2.048 MHz
$\mu$ /A-Law	Selectable	Selectable	$\mu$ -Law	A-Law	N/A	16: $\mu$ 17:A-Law
Analog Loop Back	No	Yes	No	No	No	No
Power Down Mode	Yes	Yes	Yes	Yes	Yes	Yes
Cross Talk	-80 dB	-80 dB	-80 dB	-80 dB	-70 dB	-71 dB
Idle Channel Noise Transmit/Receive	15/11 dBrcn0	15/11 dBrcn0	10 dBrcn0	-78 dBm0p	6/2 dBrcn0	15/11 dBrcn0 -75/-79 dBm0p
Gain Tracking, S/D, Frequency Response	Exceeds D3/D4 & CCITT G.712	Exceeds D3/D4 & CCITT G.712	Meets D3/D4	Meets CCITT G.712	Meets D3/D4 & CCITT G.712	Exceeds D3/D4 & CCITT G.712
Pin Count	20	24	24	22	16	16

## ISDN Components

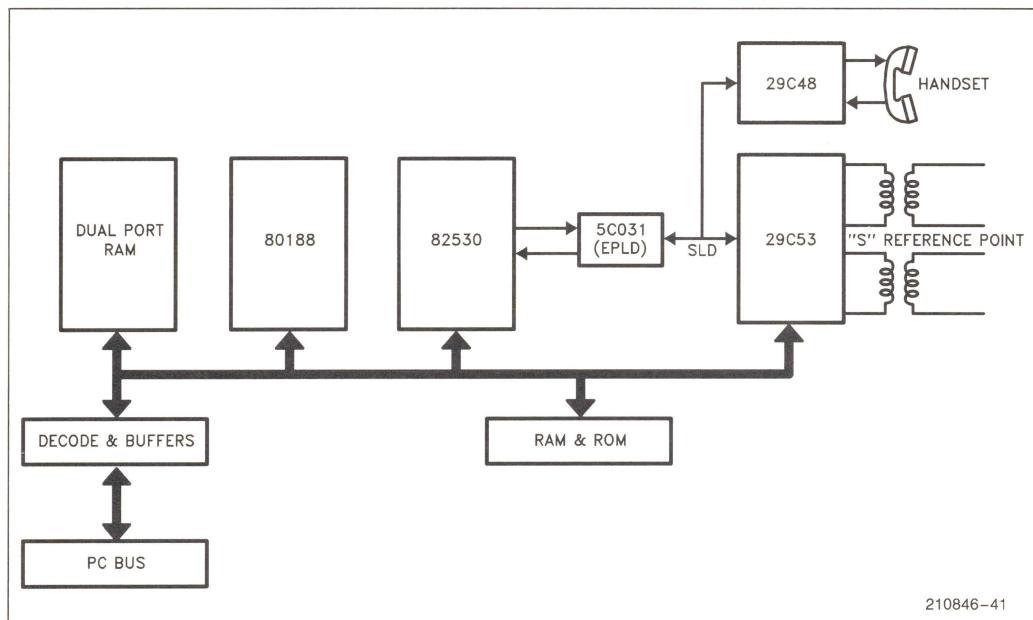
Intel's Advanced Telecom Components (iATC) architecture was conceived to insure optimum ISDN system compatibility. This means that careful consideration was given to ISDN equipment requirements on component functional partitioning. Requirements such as; application flexibility, modularity, upgrade paths, efficient interconnects, broad source of suppliers, et. al., have been factored in and are evident in the iATC architecture.

The figure below shows how the iATC family addresses the requirements in switching system equipment. In this diagram, two fundamental cards are shown: the analog line card and the digital line card. Each of the cards interface to a common backplane through a Line Card Controller (2952). The backplane carries circuit switched voice/data and control information. This interface efficiently transfers voice, data, control, and signaling/status over a three wire link consisting of a ping-pong data lead plus two clock signals.

The iATC component family provides modular building blocks for ISDN terminal applications. The 29C53 transceiver can be combined with an iATC-combo chip and appropriate microprocessor to tailor the solution to application needs.



210846-40



**Figure 19. iATC Family Addressing Terminal Requirements**

**Table 25. iATC Advanced Telecommunication Components**

Product	Description	Application	Key Features
29C48	Channel A/B program-mable combo  18 lead DIP or PLCC	Primarily for ISDN voice terminals	Selectable external balance networks Operates on channel A or B of SLD External tone injection on receive signal path
29C50A	Channel A/B program-mable combo  22 lead	Primarily for Central office and PBX sixteen subscriber per line card	Parallel 7 pin signaling interface Selectable internal and external balance networks Operates on channel A or B of SLD On-chip 3 party conferencing
29C51	High feature program-mable combo  28 lead	Primarily for Central office and PBX linecard	Parallel 10 pin signaling interface Selectable internal and external balance networks Secondary analog channels On-chip 3 party conferencing
2952	Linecard controller  40 lead	Control of subscriber circuits and data routing for analog and digital linecard applications	Connects up to 16 subscriber channels with up to 128 TDM timeslots Can operate stand alone under control of HDLC channel Can act as primary station for HDLC control channel Microprocessor port for control of all functions (optional)
29C53	I. 430 compatible four wire transceiver  28 lead DIP or PLCC	I. 430 compatible PBX linecards, terminals, terminal adaptors, network terminations	I. 430 compatible S interface Operates at either end of digital loop Bit level processing of D-channel HDLC frames

## MODEM PRODUCTS

### OVERVIEW

Paralleling the growth in the use of personal computers is the need for efficient global data communication. Intel addresses this need with the 89024 Intelligent Modem Chip Set.

In stand-alone modem applications the 89024 chip set, along with a telephone line interface (DAA) and RS232 drivers/receivers, represent all the circuitry required for implementing an auto-dial, auto-answer, sync/async, 300 to 2400 bps full duplex modem.

### Modems Features

#### 89024 INTELLIGENT MODEM CHIP SET

Intel's 89024 Intelligent Modem Chip Set is a 2400 bps full duplex modem, providing a complete system in 2 chips. It is comprised of an analog front end (89027) for filtering, and an application specific microcontroller (89026) for digital signal processing and command execution. The system conforms to the following CCITT and Bell standards for 2400/1200/600/300 bps modems:

##### CCITT

V.22 bis

V.22 A & B

V.21

##### Bell

212A

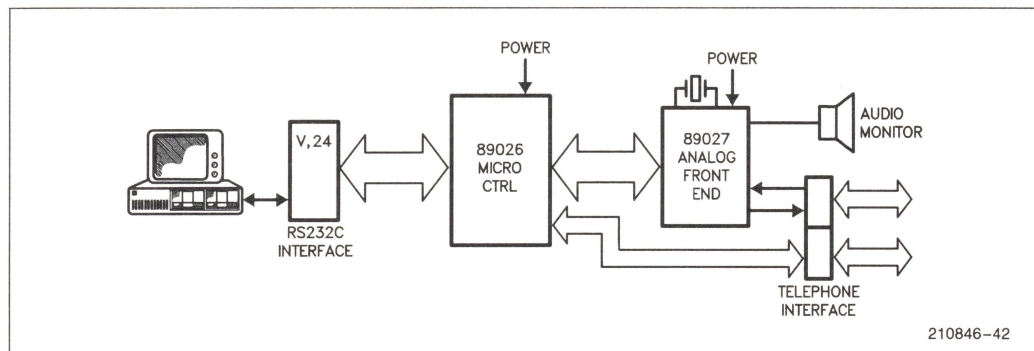
103

Main features of the 89024 include

- Built in industry standard Hayes command set
- Software customization of command and feature set
- Automatic adaptation to remote modem type (CCITT or Bell) and data rate
- Adaptive equalization
- Loopback diagnostics
- On chip hybrid and billing delay timer
- DTMF and pulse dialing, with automatic selection of dial signaling
- Dial and radial capability



The following figure shows an implementation of a fully Hayes compatible stand-alone 300 to 2400 bps modem using the 89024.



**Figure 20. 300–2400 bps Hayes Compatible Modem using Intel's Two-Chip Modem**

The high degree of integration and features offered by the 89024 greatly reduces design time, and makes it particularly suitable for applications where board space is an important consideration.

## DISTRIBUTED CONTROL MODULES

### Overview

Distributed Control Module (iDCM) products provide building blocks for construction of real-time distributed control systems based on the BITBUST<sup>™</sup> interconnect. This new serial bus architecture addresses many of the limitations inherent in traditional connection methods. For instance, future system cost reductions are limited in systems based on parallel bus structures due to their electrical and mechanical characteristics. Other traditional connection methods such as current loops and RS232C do not provide sufficient performance or flexibility for complex industrial control applications. In addition, although there are numerous industry standards for connection microprocessors, the MULTIBUS<sup>®</sup> and the STD-bus for example, there is no standard connection for microcontrollers. The BITBUS interconnect combines existing standards with new standard interfaces to provide the optimal solution for difficult distributed control problems.

The iDCM products combine hardware and software for use in applications that would benefit most from employing distributed architectures. Applications such as robotics, process control, data acquisition and control, and environmental control are a few examples.

**Table 26. Standard BITBUST<sup>™</sup> Interfaces**

Interface	Specification
Electrical	RS485
Cable	10-conductor flat ribbon or 1 to 2 wire twisted pair
Back-plane connector	64-pin Standard DIN
End-cable connector	3M #3446-1302 female
Control-board form-factor	Single-height, Double-depth Eurocard
Data Link control	Synchronous Data-link Control
Data transfer rate	62.5K baud, 375K baud and 2.4M baud
Message formats	Compatible with iDCX format command/response/status
Common command sequences	Integral Remote Access and Control (RAC) function
Operating Systems	S/W drivers for iRMX 86, 88, 286R and ISIS (for iPDS only)

### Benefits of Distributed Architectures

Distributed architectures are intrinsically more reliable than centralized architectures. In a centralized control system a central controller failure results in a system-wide failure. Distributed systems can be configured to prevent this. Also, distributed systems are more cost effective and more easily modified. For instance, performance improvements in centralized systems are expensive and do not concentrate improvements in the areas where they are needed most. In distributed systems, only the specific parts of the system that require enhancement need be modified. Most importantly, control systems based on distributed architectures have less difficulty responding to the external environment because they have less to manage.

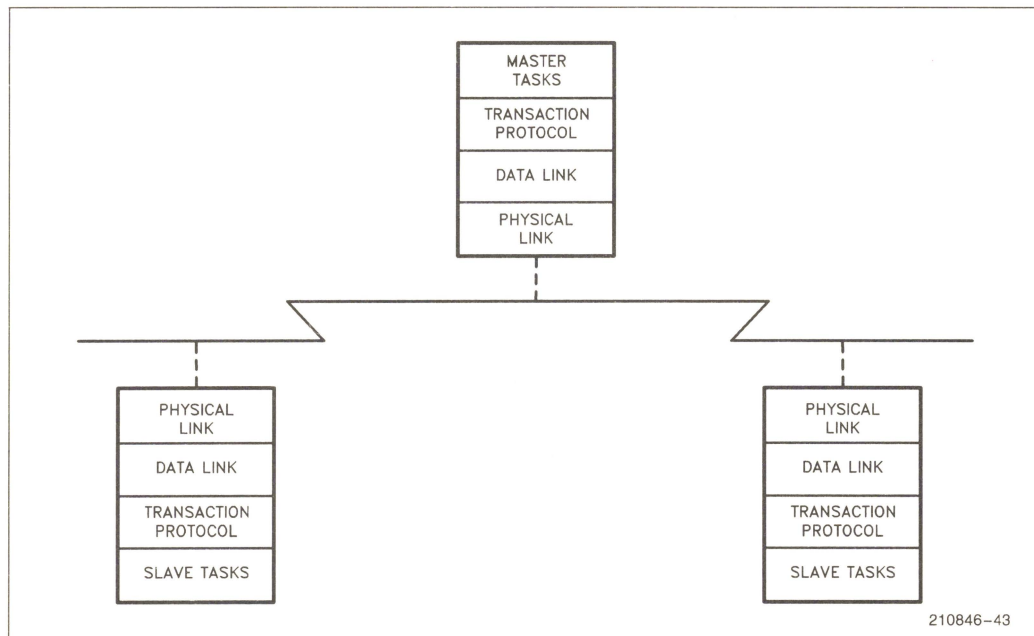


Figure 21. BITBUS™ Architecture

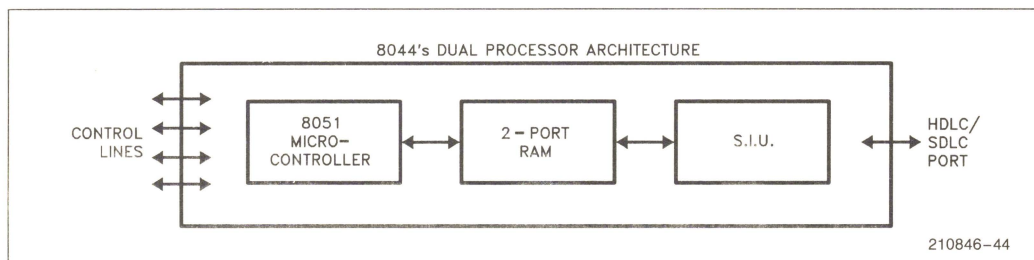


Figure 22. 8044's Dual Processor Architecture

## The BITBUS™ Interconnect

The BITBUS interconnect is a serial bus optimized for high speed transfer of short control messages in a hierarchical system. In order to provide an easy to use high performance serial interconnect, transparent to the applications programmer, high-level interfaces are specified. These interfaces include: the message structure and protocol for a multitasking environment, and a set of high-level commands for remote I/O access and application task control. As with traditional bus specifications, the electrical and data protocol levels have been defined.

Introduced in early 1984, the BITBUS microcontroller interconnect bus is Intel's newest standard. It is designed to facilitate distributed intelligent control of industrial machines and I/O such as robots, numerical control machines and process controllers. The BITBUS bus makes possible simple, high performance communications among Distributed Control Modules (DCM) and their associated MULTIBUS and PC Bus systems.

The BITBUS interconnect is based on Intel's 8044 which incorporates on a single chip the industry standard 8051 microcontroller and a high speed SDLC controller to provide fast and reliable transfer of control commands and responses. Distribution of control functions over the flexible, serial BITBUS interconnect standard will make the coordinated, automated factory more practical and cost effective.

**Table 27. BITBUS™ Products**

Product	Description
iSBX™ 344 BITBUSTM Intelligent Controller MULTIMODULE Board	<ul style="list-style-type: none"> <li>• BITBUS MULTIMODULE expansion board for MULTIBUS Single Board Computers</li> <li>• High performance 12 MHz 8044 controller</li> <li>• Integral firmware including the DCX 51 Real-Time Multitasking Executive</li> <li>• Memory sites for user's application programs</li> </ul>
PCX-344 BITBUSTM IBM PC Interface Board	<ul style="list-style-type: none"> <li>• IBM PC AT/XT "Short Slot" Form factor board interface into BITBUS iRCB boards</li> <li>• External memory sites</li> <li>• Internal Firmware optimized for Real-Time control applications on BITBUS</li> <li>• Fully compatible with Intel's MS/PC-DOS Based Development Tools</li> <li>• High Performance 8044 Single Chip Microcontroller</li> <li>• Power-up diagnostics with LED's</li> </ul>
iRCB 44/10 BITBUSTM Digital I/O Remote Controller Board	<ul style="list-style-type: none"> <li>• BITBUS standalone remote controller board with 24 programmable I/O lines</li> <li>• iSBX connector for low cost expansion</li> <li>• Eurocard formfactor</li> <li>• High performance 12 MHz 8044 controller</li> <li>• Integral firmware including the iDCX 51 Real-Time Multitasking Executive</li> <li>• Memory sites for user's application programs</li> </ul>
iRCB 44/20 BITBUSTM Analog I/O Controller Board	<ul style="list-style-type: none"> <li>• Standalone remote controller using 12MHz 8044 microcontroller</li> <li>• 16 single-ended analog input channels, <math>\pm 10V</math></li> <li>• 2 analog output channels, <math>\pm 10V</math></li> <li>• Programmable gain and 4–20 mA support</li> <li>• iSBX connector for low-cost expansion</li> <li>• Eurocard form-factor</li> <li>• Integral firmware, including iDCX 51</li> <li>• Two 28-pin memory sites, one with SRAM standard</li> </ul>
iRCX 910/920 Termination and Isolation Boards	<ul style="list-style-type: none"> <li>• iRCX-910 provides termination and electrical isolation for 24 pts of digital I/O</li> <li>• iRCX-920 provides termination and electrical isolation for 18 pts of analog I/O</li> <li>• Panel mountable or 19" rack mountable with optional mounting frame</li> <li>• Use industry standard signal conditioning modules</li> </ul>
iDCX 51 Executive	<ul style="list-style-type: none"> <li>• Real-time Multitasking Executive for the MSC-51 Microcontroller Family</li> <li>• Provides run-time scheduling services, message passing &amp; speeds development</li> <li>• Only 2.2 KBytes of code</li> </ul>
BITBUSTM Toolbox Software	<ul style="list-style-type: none"> <li>• Interactive software monitor for development and run-time</li> <li>• High performance interfaces for iRMX 86/286, iPDS, ISIS, and MS/DOS operating systems</li> </ul>



## MEMORY COMPONENTS

Intel supplies a complete line of cost effective NMOS products in volume production today with CMOS product introductions continuing through 1987.

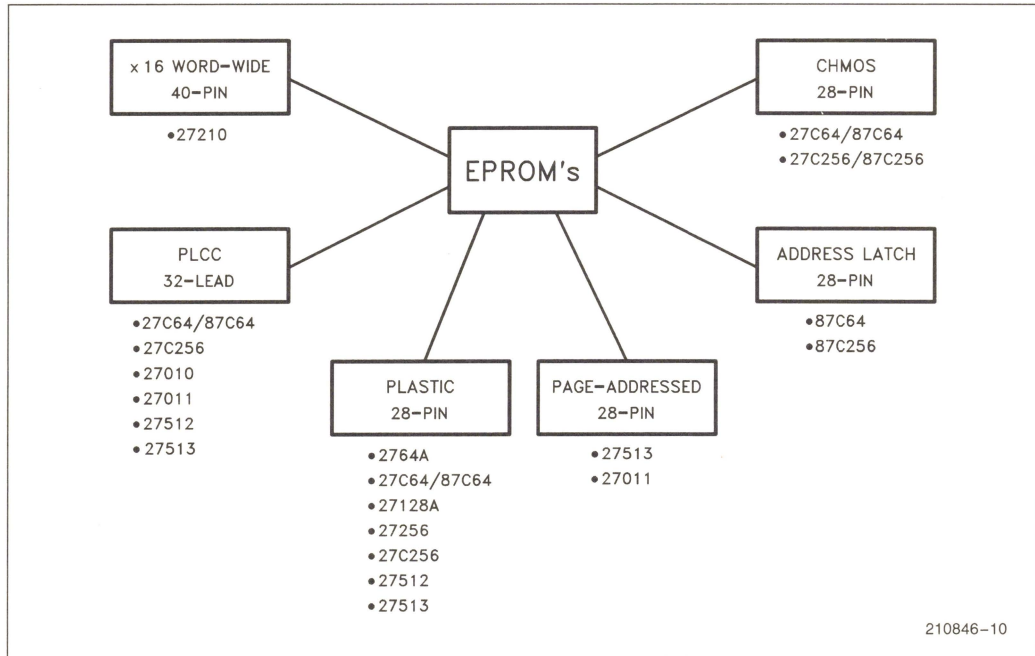


Figure 23. Enhanced EPROM Family

## EPROMS

An EPROM, or erasable, programmable read only memory, is a non-volatile memory component for program storage and prototyping applications. Intel offers a wide range of EPROM densities from 16K to 1M bits. Intel's 1Megabit compacted HMOS II-E family provides a range of design options with the X8 27010, page-addressed 27011, and X16 27210. Access times are compatible for high performance microprocessor systems. Intel has begun moving EPROMs into low power, high performance applications with its CHMOS II-E technology. CMOS versions of the popular 2764 and 27256 are now available as a 27C64 and 27C256 respectively. Latched versions for high integration solutions with microcontrollers are also available.

Intel EPROMs from the 64K density and greater feature the intelligent Programming™ Algorithm, which ensures faster and more reliable programming. Intel's Quick-Pulse Programming™ Algorithm cuts programming time down to seconds. (See Table 28.)

Intel is supporting the rapidly advancing Surface Mount Technology. Intel's line of Plastic Leaded Chip Carriers (PLCC) packages includes the 27C64, 27128A and 27C256 EPROMs. A 27512 and 1M PLCC are forthcoming in early 1987.

Table 28. EPROMs

	EPROMs													
	2722A	2764A	27128A	27128B	27256	27512	27513	27010	27011	27210	27064	87C64	27C256	87C256
Size (bits)	32K	64K	128K	128K	256K	512K	512K	1024K	1024K	1024K	64K	64K	256K	256K
Organization	4K x 8	8K x 8	16K x 8	16K x 8	32K x 8	512K x 8	4 x 16K x 8	128K x 8	8 x 16K x 8	64K x 16	8K x 8	8K x 8	32K x 8	32K x 8
# of Pins	24	28	28	28	28	28	28	32	28	40	28	28	28	28
Read Access (ns)	200-450	200-300	150-300	110-150	170-300	200-300	200-300	200-300	200-300	150-250	150-300	150-300	170-300	170-300
Programming Time (Typical)*	3.5 min.	1 sec.	3 sec.	3 sec.	6 sec.	12 sec.	12 sec.	20 sec.	20 sec.	10 sec.	1 sec.	1 sec.	6 sec.	6 sec.
Quick-Pulse Programming™	—	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Current (mA)	Active	Active	Active	Active	Active	Active	Active	Active	Active	Active	Active	Active	Active	Active
	Standby	Standby	Standby	Standby	Standby	Standby	Standby	Standby	Standby	Standby	Standby	Standby	Standby	Standby
Express Available	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Military Available	Yes	Yes	Yes	Yes	Yes	Yes	—	—	—	—	Yes	—	Yes	—
Failure Rate/1000 Hrs. @ 55°C (60% UCL)	<.02%	<.02%	<.02%	<.02%	<.02%	<.02%	<.02%	<.02%	<.02%	<.02%	<.02%	<.02%	<.02%	<.02%
Reliability Data Literature #	RR-35D	RR-35D	RR-35D	—	RR-35D	RR-35D	RR-35D	RR-35D	RR-35D	RR-35D	RR-35D	RR-35D	RR-35D	RR-35D
Plastic	Yes	Yes	Yes	—	Yes	Q187	Q187	—	—	—	Yes	Yes	Yes	—
PLCC	—	—	Yes	—	—	Q386	Q386	Q187	—	Q187	Yes	Yes	Yes	—
On-Chip Latch	No	No	No	No	No	No	No	No	No	No	No	Yes	No	Yes

\*EPROMs per device.

**Table 29. SRAMs**

	HMOS* Static RAMs					CHMOS* Static RAMs	
Part Number	2114A	2115/ 2125A	2147H	2148H	2149H	51C67	51C68
Size (Bits)	4K	1K	4K	4K	4K	16K	16K
Organization	1K x 4	1K x 1	4K x 1	1K x 4	1K x 1	16K x 1	4K x 4
# of Pins	18	16	18	18	18	20	20
Read Access (ns)	100–250	45–70	35–70	45–70	45–70	30–35	30–35
Maximum Current dis (mA) (Operating/ Standby)	40–70	75–125	140–180/ 10–30	125–180/ 20–30	125–180	60–55/5 60–80/5–10	60–80/5–10
Express Available	Yes	Yes	Yes	Yes	Yes	—	—
Military Available	Yes	No	Yes	Yes	No	Yes	Yes
Failure Rate/ 1000 Hrs. @ 55° (60% UCL)	0.007%	0.017%	0.009%	0.009%	0.009%	TBD	TBD
Reliability Data Literature #	—	—	RR-26	RR-26	RR-26	—	—

\*CHMOS and HMOS are patented processes of Intel Corporation.

## E<sup>2</sup>PROMs

As part of its non-volatile memory offerings, Intel produces a family of electrically erasable programmable ROMs (E<sup>2</sup>PROMs). These devices are characterized by fast read access, in-circuit alterability, and non-volatile data retention.

For years, E<sup>2</sup>PROMs have been the preferred approach for data tabling applications—the storage of calibration constants, user-defined functions, price tables, or accumulated totals. As densities have increased, E<sup>2</sup>PROMs have penetrated code storage applications. Where field updates to system firmware are expected, E<sup>2</sup>PROMs facilitate remote revision over a phone line. Or, in networked equipment, new program code may be downloaded from the host system over a telecom/datacom link. E<sup>2</sup>PROMs eliminate the traditional board swapping and rework associated with firmware changes, thus E<sup>2</sup>PROMs offer a means to cut rising service costs and inventory expenses.

E<sup>2</sup>PROMs are furnished in JEDEC-approved byte-wide DIP and chip carrier packages, for both commercial and military applications. Extended temperature and burn-in (EXPRESS Program) versions are also available.

**Table 30. E<sup>2</sup>PROMs**

	<b>E<sup>2</sup>PROMs</b>		
	<b>2864A</b>	<b>2817A</b>	<b>2816A</b>
Size (Bits)	64K	16K	16K
Organization	8K x 8	2K x 8	2K x 8
# of Pins	28	28	24
Read Access (ns)	200-350	200-350	200-350
Write Speed (ms)	10	10-20	15
Page Mode Write	16 Bytes	No	No
On-Chip Latches	Yes	Yes	No
On-Chip Write Timing	Yes	Yes	No
Current: Active (mA)	140	100	100
Standby (mA)	60	45	50
Express Available	Yes	Yes	Yes
Military Available	Yes	Yes	No
Failure Rate/1000 Hrs @55°C (60% UCL)	.0309%	.117% .117%	.013% .0132%
Reliability Literature	RR-59A	RR-59A	RR-59A
Cerdip	Yes	Yes	Yes
Plastic	Q1'87	Yes	No
PLCC (32-Lead)	Q1'87	Yes	No

## **Megabit EPROM Architecture: Continuity from Today; A Foundation for Tomorrow**

Today, as EPROM density has evolved to the one-million bit density level, semiconductor manufacturers and system designers alike face an architectural and technology turning point. Current EPROM users have adopted the 28-pin site as the standard footprint for devices from 64-kilobit through 512-kilobit densities. To maintain design continuity for customers seeking increased density, this 28-pin site must now be made to accommodate the one-megabit EPROM. Intel Corporation is committed to maintaining design continuity for its customers, through both its architecture and technology. Intel offers three versions of its one-megabit EPROM—two that build on the past, all three pave the way to the future.

### **27011—Page-Addressed (8 x 16K x 8) EPROM**

This device enables firmware-intensive designs to be based on 8-bit microprocessors and microcontrollers. Many of these popular processors and controllers are limited in their addressing capabilities and could not otherwise take advantage of one megabit of EPROM memory. With this EPROM architecture, new designs based on 8-bit or 16-bit microprocessors can utilize the page-addressing feature, allowing for software upgrades without board re-design. The entire chip looks to the system like eight 128-kilobit EPROMs in the space of one 128-kilobit EPROM. Inventive system designers are finding that advanced software features prolong the usefulness of their 8-bit microprocessor-based system and their software investment. For existing systems constrained to a 28-pin socket, page-addressing provides the only 28-pin solution at the 1-megabit density.

Intel's 27011 one-megabit page-addressed EPROM is configured 8 pages of 16 kilobytes each (8 by 16K by 8). It consumes the least amount of board space among all megabit EPROMs. The by-8 page-addressed architecture is the only no-hardware-change upgrade path, conserving the 28-pin site up to the 32-megabit density.



## 27210—Word-wide (64K x 16) EPROM

With its word-wide megabit EPROM pinout, Intel has broken with the past to offer a simplified pinout, one that is a logical extension from the 28-pin and 32-pin EPROM footprints and applicable to both 16-bit and 32-bit microprocessor-based systems. Its word-wide organization makes the 27210 EPROM particularly suited to 16-bit microprocessor applications. All addresses are on one side of the device and data on the other, making this architecture a simple solution that meets the needs of today's advanced microprocessors. This approach preserves performance while simplifying board layout design.

## 27010—Byte-wide (128K x 8) EPROM

The standard-addressed-by-8 configuration takes the same step from the 28-pin family as the first 28-pin configuration took from the standard 24-pin site in 1980. It is an extension of the mainstream EPROM market today. Its upward and backward compatibility with other densities gives customers the flexibility to accommodate code overruns or to upgrade their systems to take advantage of the most cost-effective density. For larger, standard-addressed memory arrays of 16-bit or 32-bit words, the smaller 32-pin DIP sockets use less board space than the 40-pin DIP alternatives. This concept allows pin-compatible growth through the 8-megabit density.

Customers can prepare to take advantage of future densities today. Using 32-pin sockets, customers can design with the 27512 EPROM today while establishing an upgrade path to the future as one-megabit EPROMs become cost-effective in 1987.

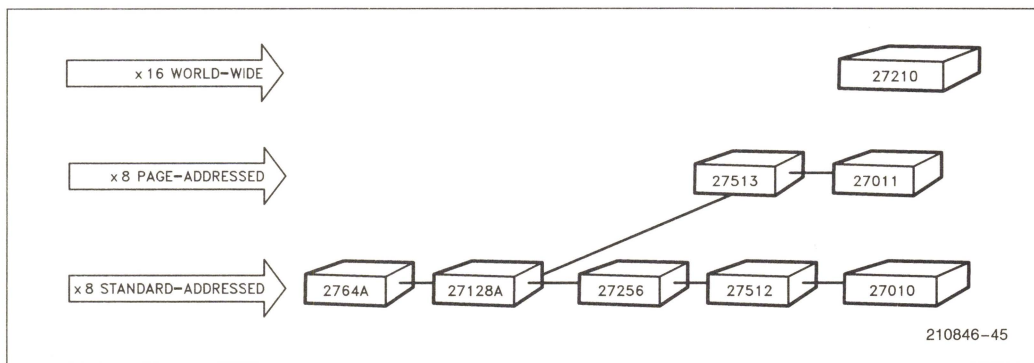


Figure 24. Intel's Pinout Evolution

## EMBEDDED CONTROLLERS

Intel offers four basic families of Embedded Controllers; general purpose 8-bit, advanced 8-bit, advanced 16-bit and 16-bit High Integration devices. The relative range of application performance is indicated in the diagram below.

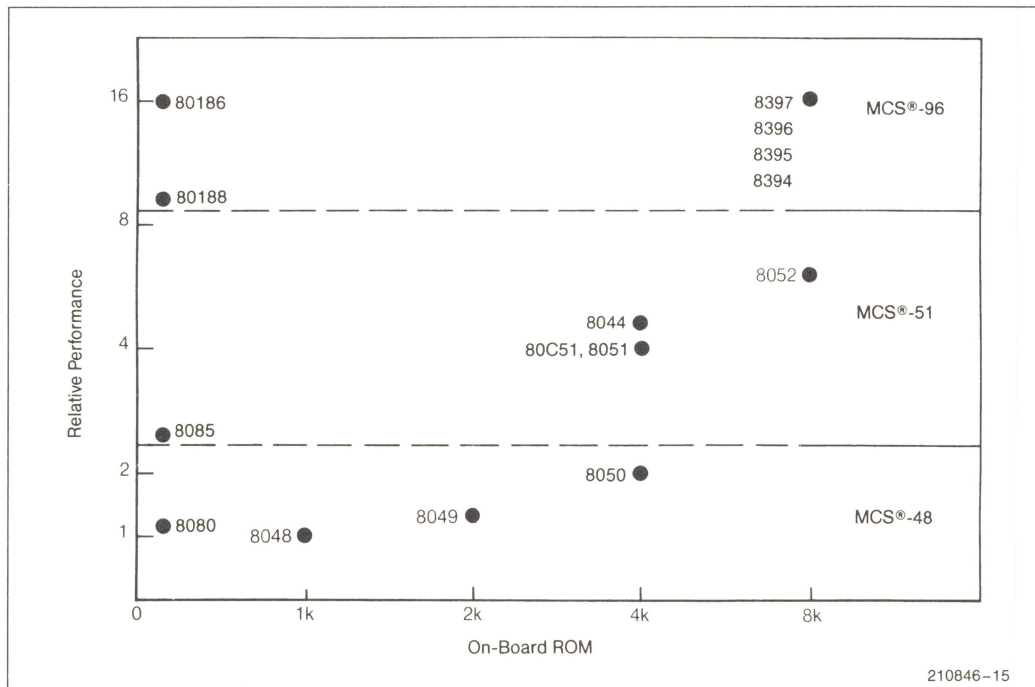


Figure 25. Embedded Controller Performance

### BASIC FAMILY CHARACTERISTICS

**MCS®-48:** Designed for general purpose 8-bit control applications.

Average instruction time — 2.0  $\mu$ s

Maximum addressable code — 4 Kbytes

**MCS-51:** Designed for advanced 8-bit control applications.

Typical instruction cycle time — 1.0  $\mu$ s (byte operations); 0.75  $\mu$ s for high speed CHMOS

Hardware multiply and divide (4  $\mu$ s — byte by byte multiply)

Full duplex asynchronous serial port

On-chip Boolean Processor

Maximum addressable code — 64 Kbytes

**MCS-96:** Designed with 16-bit processing power for complex algorithms.

Average instruction time — 1.25  $\mu$ s (word operations)

Hardware multiply and divide (6.5  $\mu$ s — word by word multiply)

Analog and high speed programmable digital I/O

Full duplex asynchronous serial port

Maximum addressable code — 64 Kbytes

10-bit 8 channel A/D converter

- 8080/8085: This product line is the industry standard for first generation 8-bit computing with five second sources and a 9-year track record of production and availability. The 8085A has kept up with advances in silicon technology and is now manufactured as the 8085AH on Intel's state-of-the-art HMOS process.
- 80186/80188: These parts are highly integrated versions of the 8086 microprocessor intended for data control applications. They combine 15 to 20 of the most common 8086 system components onto one device. Included with the CPU is the clock generator, an interrupt controller, timers, DMA channels and chip select logic. The 80186 operates on a 16-bit bus and the 80188 operates on an 8-bit bus. Both parts operate on a 16-bit bus internally.

## GENERAL PURPOSE 8-BIT EMBEDDED CONTROLLERS

Intel's MCS-48 family of 8-bit embedded controllers has become a world standard. They are available in several versions: with on board ROM, on board EPROM, or CPU only, to better fit your specific application needs. MCS-48 products are now fabricated on Intel's advanced HMOS II.

**Table 31. General Purpose Embedded Controllers**

ROM Version	8048AH	8049AH	8050AH
EPROM Version	8748H	8749H	—
CPU/RAM/I/O	8035AHL	8039AHL	8040AHL
Cycle Time	1.36 $\mu$ s	1.36 $\mu$ s	1.36 $\mu$ s
RAM Memory (Bytes)	64	128	256
Program Memory (Bytes)	1K	2K	4K
I/O Lines	27	27	27
SYNC Mode	Yes	Yes	Yes
Timer-Counter	1	1	1
A/D	—	—	—
Interrupts	2	2	2
Program Limit	4K	4K	4K
Ext Data Limit (Bytes)	256	256	256
Development Support	See Development Tools, Page 20, and Software, Page 109.		

## ADVANCED 8-BIT EMBEDDED CONTROLLERS

Intel's MCS-51 family is the industry standard for 8-bit high performance microcontrollers. The family architecture is optimized for control oriented and real-time processing applications. They are available in several versions—with on-board ROM, on-board EPROM, and CPU only to better fit your specific application needs. MCS-51 products are available either on Intel's advanced HMOS or CHMOS III processes offering higher performance and reliability while consuming less power.

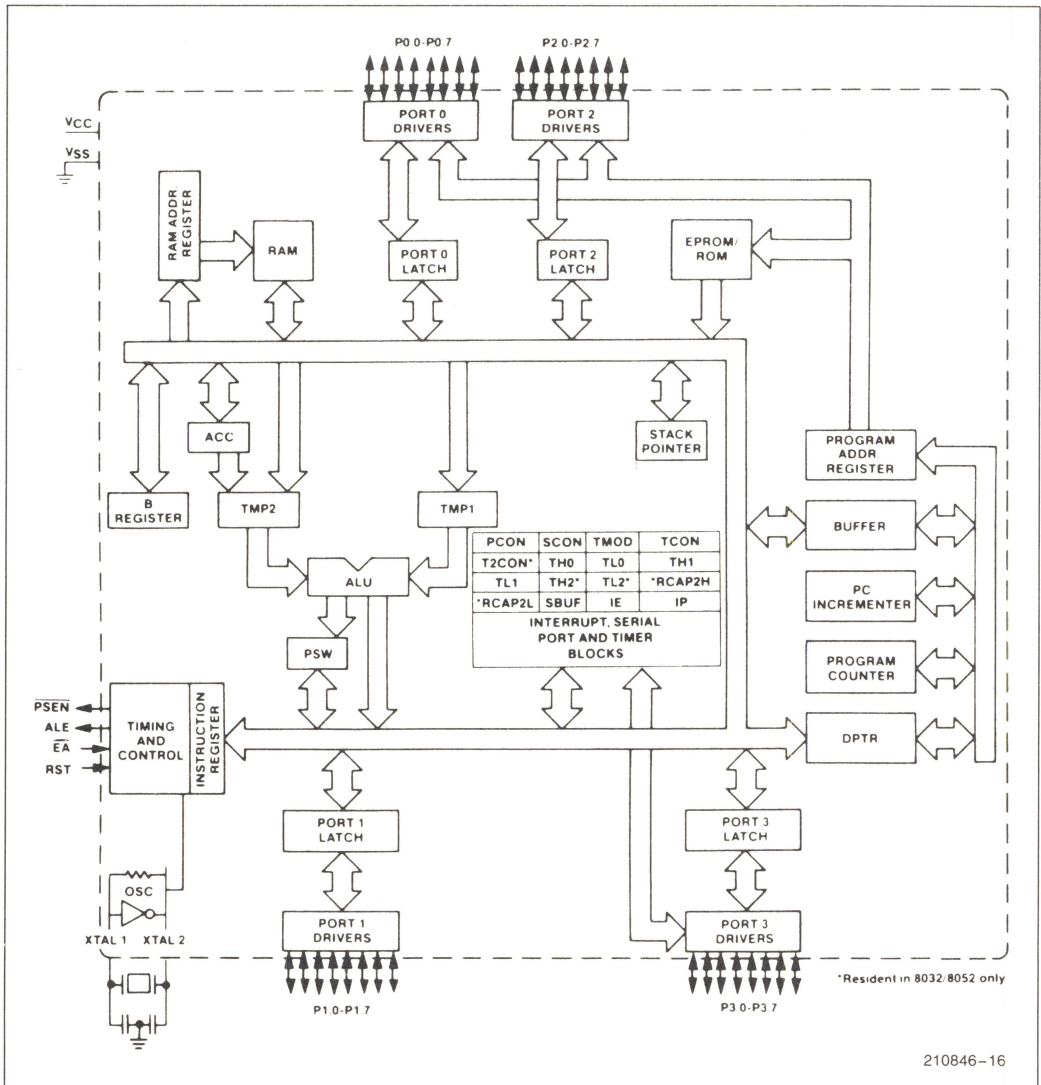


Figure 26. MCS®-51 Block Diagram



**Table 32. Advanced 8-Bit Embedded Controllers**

Feature	8051AH	8031AH	8751H	80C51BH	80C31BH	87C51	8052AH	8032AH	8752	8044H‡
Program Memory (Bytes)	4K	—	4K EPROM	4K	—	4K EPROM	8K	—	8K EPROM	4K
RAM Memory (Bytes)	128	128	128	128	128	128	256	256	256	192
Program Memory Expansion (Off Chip) (Bytes)	64K	64K	64K	64K	64K	64K	64K	64K	64K	64K
Data Memory Expansion (Off Chip) (Bytes)	64K	64K	64K	64K	64K	64K	64K	64K	64K	64K
Max. Clock Frequency (MHz)	12	12	12	16	16	16	12	12	12	12
Typical Instruction Time (μs)	1	1	1	.75	.75	.75	1	1	1	1
16-Bit Timer/Counters	2	2	2	2	2	2	3	3	3	2
Serial Communications	Synchronous Mode Asynchronous Modes, 9 or 10-Bit Programmable									HDLC/SDLC
No. of I/O Lines	32	16	32	32	16	32	32	16	32	32
Interrupt Sources (Two Priority Levels)	5	5	5	5	5	5	6	6	6	5
Power Requirements (ICC MAX mA)	125	125	250	24	24	29	175	175	175	200
Programmable Power Modes Idle Power Down	—	—	—	4.0 mA 50 μA	4.0 mA 50 μA	4.0 mA 50 μA	—	—	—	— 30 mA
Development Support	See Development Tools, Page 20, and Software, Page 109.									

\*Products designated with a "C" (i.e., 80C51BH) are CMOS devices.

‡For details refer to Page 42, Table 21.

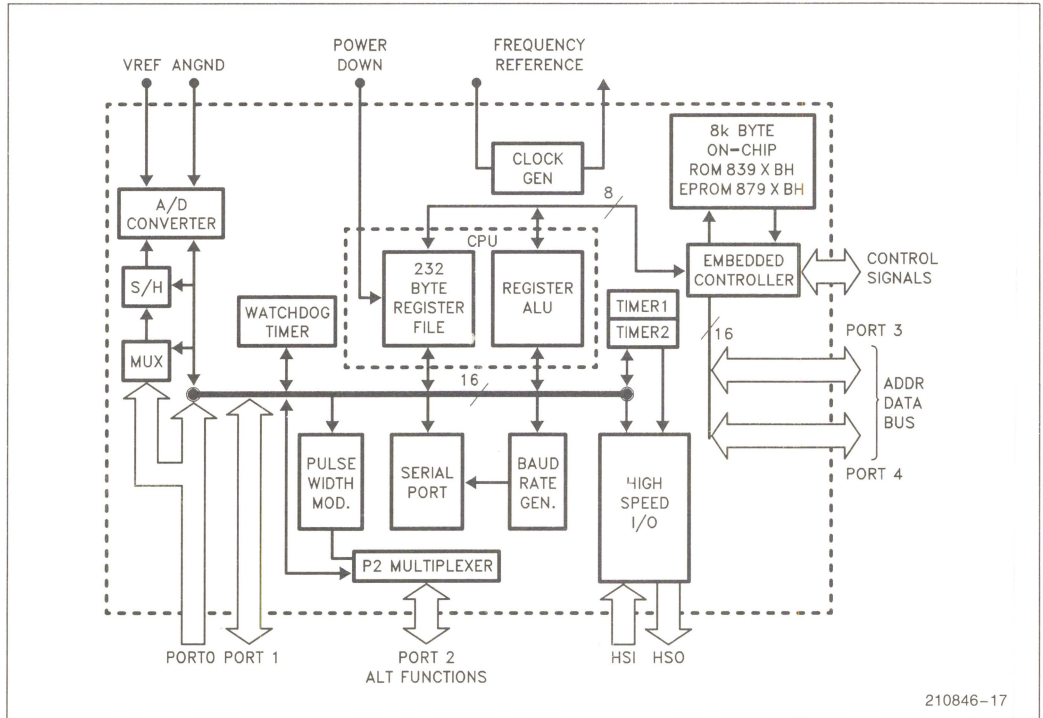


Figure 27. MCS®-96 Block Diagram

## ADVANCED 16-BIT EMBEDDED CONTROLLERS

Intel's MCS-96 family is based on the state-of-the-art 8096 device. This 16-bit Embedded controller offers the highest level of systems integration ever achieved on a single chip controller. The 8096 provides board level performance through a wide range of sophisticated I/O facilities and peripherals integrated onto the same piece of silicon with a powerful 16-bit CPU. The integration of these subsystems offers a single chip solution to many control problems which have previously required multiple chip solutions. Development support includes high-level language support, assembler support and emulation hardware support. The list of main features includes:

- 232 Byte Register File
- Register-to-Register Architecture
- 10-Bit A/D Converter with S/H
- Five 8-Bit I/O Ports
- 20 Interrupt Sources
- Pulse-Width Modulated Output
- Dedicated Baud Rate Generator
- Run-Time Programmable EPROM
- High Speed I/O Subsystem
- Full Duplex Serial Port
- 6.25  $\mu$ s 16 x 16 Multiply
- 6.25  $\mu$ s 32/16 Divide
- 16-Bit Watchdog Timer
- Four 16-Bit Software Timers
- Two 16-Bit Counter/Timers
- ROM/EPROM Security
- Dynamically Reconfigurable 8-Bit or 16-Bit Bus Width

**Table 33. Advanced 16-Bit Embedded Controllers**

		Without A/D	With A/D
ROMless	48 Pin	C8094BH - Ceramic DIP P8094BH - Plastic DIP	C8095CH - Ceramic DIP P8095BH - Plastic DIP
	68 Pin	A8096BH - Ceramic PGA N8096BH - PLCC	A8097BH - Ceramic PGA N8097BH - PLCC
ROM	48 Pin	C8394BH - Ceramic DIP P8394BH - Plastic DIP	C8395BH - Ceramic DIP P8395BH - Plastic DIP
	68 Pin	A8396BH - Ceramic PGA N8396BH - PLCC	A8397BH - Ceramic PGA N8397BH - PLCC
EPROM	48 Pin	C8794BH - Ceramic DIP	C8795BH - Ceramic DIP
	68 Pin	A8796BH - Ceramic PGA R8796BH - Ceramic LCC	A8797BH - Ceramic PGA R8797BH - Ceramic LCC

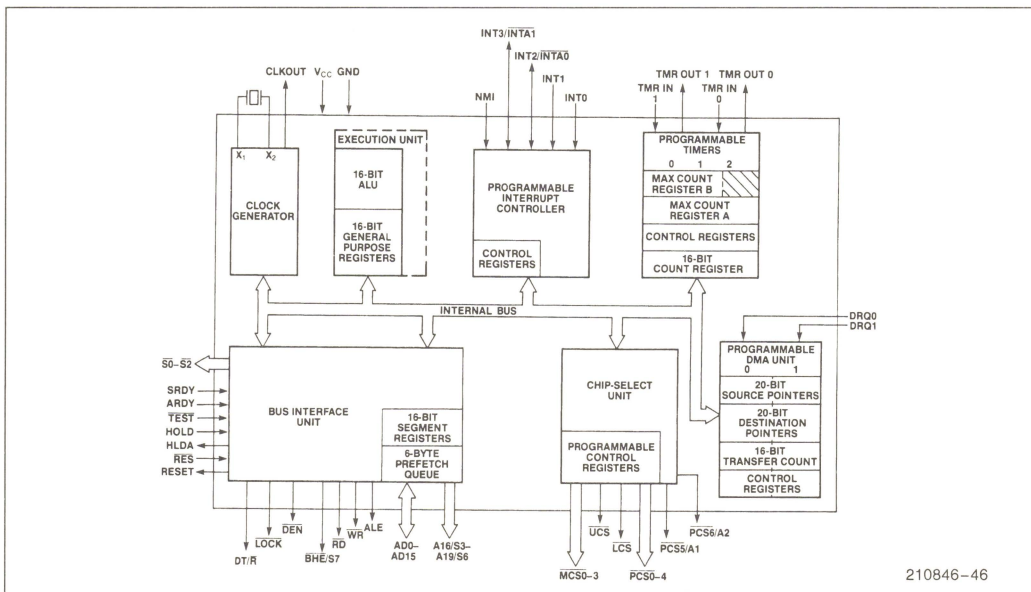
## 80186 HIGH INTEGRATION EMBEDDED CONTROLLER

The 80186 family of Embedded Controller was designed to bring the 8086 architecture to embedded control applications. Six of the most often used functions of an 8086 system have been integrated onto a single chip. Along with higher integration, the 80186 offers higher performance than the standard 8086 via detailed improvements to the design. The 80186 family consists of two Embedded Controllers; the 80186 and the 80188. These processors have identical capabilities except that the 80186 operates on a 16-bit bus while the 80188 operates on an 8-bit bus. The 80186 offers higher system performance with its 16-bit bus; the 80188 offers lower system cost with its 8-bit bus. Both controllers operate internally with a 16-bit bus and generate a 20-bit address to give a total address space of 1 Megabyte.

The major features of the 80186 and 80188 include:

- 2 Channel DMA (Direct Memory Access) unit
- 3 16-bit timer/counters
- Interrupt controller
- Clock generator
- Chip select logic
- Ready control logic

Unlike the other embedded control products, the 80186 is intended for applications which need relatively large amounts of program storage and require large and complex data structures. Since it is impractical to integrate the amount of memory required for typical applications onto the processor chip, no attempt is made to incorporate memory on board.



**Figure 28. 80186 Block Diagram**

## AUTOMOTIVE

Although Intel has been a leader in VLSI since 1968, our partnership with the automotive industry didn't begin until 1978. By working closely with automotive engineers and designers, we succeeded in adapting our industry standard 8-bit microcontroller to meet the requirements for "in-vehicle" applications.

Shortly thereafter, under the guidance of several automotive manufacturers and suppliers, we developed a 16-bit microcontroller designed specifically for automotive applications. Today, our A8096 is the automotive industry's most widely accepted 16-bit electronic engine controller.

Our partnership with automotive engineering trendsetters has also led to the use of our 8- and 16-bit microcontrollers and memories in anti-lock brake systems, traction control, dynamic suspensions, cruise controls and electric steering.

In-vehicle networks, driver information devices and a myriad of safety and convenience applications are also emerging as promising areas for Intel's products.

In the future, electronic logic and control will be instrumental in helping the auto industry meet the demands for higher performance and increased efficiency at lower cost.

**Table 34. Automotive Memories Product Line**

<b>EPROMs</b>			
<b>Part Number</b>	<b>Process</b>	<b>Memory Size</b>	<b>Package Type</b>
AD27C64	CHMOS	64K (8K x 8)	28L Cerdip
AN27C64	CHMOS	64K (8K x 8)	32L PLCC
AP27C64	CHMOS	64K (8K x 8)	28L Plastic Dip
AD27128A	NMOS	128K (16K x 8)	28L Cerdip
AD27C256	CHMOS	256K (32K x 8)	28L Cerdip
AD87C256	CHMOS	256K (32K x 8 Latched)	28L Cerdip
"A" Spec: -40°C to +125°C			
"B" Spec: -40°C to +125°C, 168 Hour Burn-in			
<b>E<sup>2</sup>PROMs</b>			
AD2817A	NMOS	16K (2K x 8)	28L Cerdip
AP2817A	NMOS	16K (2K x 8)	28L Plastic Dip
AD2864A	NMOS	64K (8K x 8)	28L Cerdip
Temperature Range: -40°C to +105°C			
<b>NVRAM</b>			
TD2001	HMOS-E	1K (128 x 8)	18L Cerdip
TD2004	HMOS-E	4K (512 x 8)	28L Cerdip
Temperature Range: -40°C to +85°C			



**Table 35. Automotive Embedded Controller Product Line**

Part Number	Features	Package Type
A8051	8-Bit, 4K ROM, 128 Bytes RAM	40 Pin Plastic DIP, Cerdip 44 Pin PLCC
A8031	8-Bit, 128 Bytes RAM	40 Pin Plastic DIP, Cerdip 44 Pin PLCC
A8751	8-Bit, 4K EPROM, 128 Bytes RAM	44 Pin LCC 40 Pin Cerdip
A8052	8-Bit, 8K ROM, 256 Bytes RAM	40 Pin Plastic DIP, Cerdip
A8032	8-Bit, 256 Bytes RAM	40 Pin Plastic DIP, Cerdip
A80C51	8-Bit, 4K ROM, 128 Bytes RAM, CHMOS	40 Pin Plastic DIP, Cerdip 44 Pin PLCC
A80C31	8-Bit, 128 Bytes, RAM, CHMOS	40 Pin Plastic DIP, Cerdip 44 Pin PLCC
A8397	16-Bit, 8K ROM, 232 Bytes RAM, A/D	68 Pin PLCC, PGA, Plastic Flatpack
A8097	16-Bit, 232 Bytes RAM, A/D	68 Pin PLCC, PGA, Plastic Flatpack
A8096	16-Bit, 232 Bytes RAM	68 Pin PLCC, PGA, Plastic Flatpack
A8396	16-Bit, 8K ROM, 232 Bytes RAM	68 Pin PLCC, PGA, Plastic Flatpack
A8095	16-Bit, 232 Bytes RAM, A/D	48 Pin DIP
A8395	16-Bit, 8K ROM, 232 Bytes RAM, A/D	48 Pin DIP
A8094	16-Bit, 232 Bytes RAM	48 Pin DIP
A8395	16-Bit, 8K ROM, 232 Bytes RAM	48 Pin DIP

Temperature Ranges: HMOS – 40°C to 110°C Ambient

CHMOS – 40°C to + 125°C Ambient

Packages: DIP = Dual-In-Line Package

Cerdip = Ceramic Dual-In-Line Package

LCC = Leaded Chip Carrier

PLCC = Plastic Leaded Chip Carrier

## MILITARY PRODUCTS

The components included in Intel's Military product family are summarized in the table below. A more complete description of each generic device can be found in this Guide by referring to the appropriate component section or by using the Alphanumeric Index located in the front of this Guide.

**Table 36. Military Products**

Type	Product	Description	Maximum Clock Speed	Package Type			
				DIP	LCC	PGA	CQ
Embedded Controller	M8031AH	High-Performance 8-Bit Single-Chip Computer without ROM, 128 × 8-Bit RAM, Boolean Processor	12 MHz	X	X		
	M80C31BH	High-Performance 8-Bit Single-Chip Computer without ROM, 128 × 8-Bit RAM, Low Power CHMOS, Power-Down and Idle Modes	12 MHz	X	X		
	M8035AHL	8-Bit Single-Chip Computer without ROM, 64 × 8-Bit RAM, Power-Down Mode	11 MHz	X			
	M8048AH	8-Bit Single-Chip Computer, 1K × 8-Bit Mask Programmable ROM, 64 × 8-Bit RAM, Power-Down Mode	11 MHz	X			
	M8051AH	High-Performance 8-Bit Single-Chip Computer, 4K × 8-Bit Mask Programmable ROM, 128 × 8-Bit RAM, Boolean Processor	12 MHz	X	X		
	M80C51BH	High-Performance 8-Bit Single-Chip Computer, 4K × 8-Bit Mask Programmable ROM, 128 × 8-Bit RAM, Low Power CHMOS, Power-Down and Idle Modes	12 MHz	X	X		
	M8085AH	8-Bit Parallel CPU, 1.3 μsec Instruction Cycle, On-Chip Clock Generator and System Controller, DESC SID 7901001QX	3 MHz	X			
	M8097	High-Performance 16-Bit Embedded Controller with A/D, PWM Output, HSIO, 232 Bytes RAM, 40 I/O Lines, Watch Dog Timer	12 MHz			X	X
	M80186	High Integration	6, 8 MHz			X	X
	M8397	16-Bit Embedded Controller	12 MHz			X	X
	M8748H	High-Performance 16-Bit Embedded Controller with A/D, PWM Output, HSIO, 232 Bytes RAM, 40 I/O Lines, Watch Dog Timer, plus 8K × 8-Bit ROM	12 MHz			X	X
	M8751H	8-Bit Single-Chip Computer with 1K × 8-Bit EPROM, 64 × 8-Bit RAM	11 MHz	X			
	M87C51	High-Performance 8-Bit Single-Chip Computer with 4K × 8-Bit EPROM, 128 × 8-Bit RAM, Boolean Processor	8 MHz	X	X		
		High-Performance 8-Bit Single Chip Computer with 4K × 8-Bit EPROM, 128 × 8-Bit RAM, Low Power CHMOS, Power-Down and Idle Modes	12 MHz	X	X		

**Table 36. Military Products (Continued)**

Type	Product	Description	Maximum Clock Speed	Package Type			
				DIP	LCC	PGA	CQ
Embedded Controller (Continued)	M8797	High-Performance 16-Bit Embedded Controller with A/D, PWM Output, HSIO, 232 Bytes RAM, 40 I/O Lines, Watch Dog Timer, Plus 8K × 8-Bit EPROM	12 MHz			X	X
Microprocessor	J8080A	8-Bit Parallel CPU, 2 μsec Instruction Cycle, (JAN) M38510/42001 BQX	2 MHz	X			
	J8086	16-Bit Microprocessor, (JAN) M38510/53001BQX	5 MHz	X			
	M8086	16-Bit Microprocessor	5 MHz, 8 MHz	X	X		
	M8087	Numeric Data Processor, Math and Floating Point Hardware for Host M8086 and M8088	5 MHz	X			
	M8088	High-Performance 8-Bit Microprocessor, 16-Bit Internal Architecture	5 MHz	X			
	M80286	High-Performance 16-Bit Microprocessor with Memory Management and Protection	6, 8 MHz			X	X
	M80287	Numeric Processor Extension, Math and Floating Point Hardware Support for Host M80286 (6, 8 MHz)	6 MHz	X			
	M80C86	16-Bit CHMOS Microprocessor	5 MHz	X			
	M80386	32-Bit CHMOS Microprocessor	12.5, 16 MHz			X	X
	M80387	Numeric Processor for M80386	12.5, 16 MHz			X	
Support Product	M8224	Single-Chip Clock Generator and Driver for M8080A		X			
	M8228	Single-Chip System Controller and Driver for M8080A		X			
	M8243	I/O Expander for M8035AHL/M8048AH/M8748H		X			
	M8282	8-Bit Parallel Address/Data Latch		X	X		
	M8283	8-Bit Parallel Inverting Address/Data Latch		X	X		
	M8284A	Single-Chip Clock Generator and Driver for M8086, M8088, M8087 and M8089	8 MHz	X	X		
	M8266	8-Bit Parallel Address/Data Bus Transceiver		X	X		
	M8287	8-Bit Parallel Inverting Address/Data Bus Transceiver		X	X		
	M8288	Bus Controller for M8086, M8088 and M8089, Provides Command and Control Timing Generation	8 MHz	X	X		
	M8289	Bus Arbiter for M8086, M8088 and M8089 System Busses	8 MHz	X	X		
	M82188	Integrated Bus Controller For use with M8086, M8088, and M80186-6 Systems	8 MHz	X			

**Table 36. Military Products (Continued)**

Type	Product	Description	Maximum Clock Speed	Package Type			
				DIP	LCC	PGA	CQ
Support Product	M82C84A5	CHMOS Clock Generator and Driver for M80C86	5 MHz	X			
	M82C88	CHMOS Bus Controller for M80C86	5 MHz	X			
	M82284	Clock Generator and Ready Interface for M80286	6, 8 MHz	X			
	M82288	Bus Controller for M80286	6, 8 MHz	X			
	M82289	Bus Arbiter for M80286	6, 8 MHz	X			
	M82384	Clock Generator and Ready Interface for M80386	12.5, 16 MHz	X			
	M82258	Advanced DMA Controller for 80286		X			
Controller	M8257	4-Channel Programmable DMA (Direct Memory Access) Controller for M8080A and M8085AH	3 MHz	X			
	M8259A	Programmable Interrupt Controller, Handles Up to 8-Vectored Priority Interrupts		X	X		
Peripheral	M8155	256 × 8-Bit Static RAM with 22 Programmable I/O Ports, Binary Timer/Counter		X			
	M8185	1K × 8-Bit Static RAM with Internal Address Latch		X			
	M8231A	Arithmetic Processing Unit, High-Performance Fixed and Floating Point Arithmetic and Floating Point Trigonometric Operation	4 MHz	X	X		
	M8251A	Programmable Communication Interface, (USART)	3 MHz	X	X		
	M8254	Programmable Interval Timer, 3 Independent 16-Bit Counters	DC to 8 MHz	X	X		
	M8255A	Programmable Peripheral Interface, 24 Programmable I/O Ports		X	X		
	M8274	Multi-Protocol Serial Controller	880 Kbps	X			
	M82720	Graphics Display Controller	4 MHz	X			
	M8744	High Performance 8-Bit Microcontroller with On-Chip Serial Communication Processor	10 MHz/ 2.4 mbps	X			
	M82C54	CHMOS, 3 16-Bit Counters	8 MHz	X			
		8254 Compatible					
	M82C55	CHMOS, 24 TTL Compatible Parallel I/O Lines		X			



**Table 36. Military Products (Continued)**

Type	Product	Description	Maximum Clock Speed	Package Type		
				DIP	LCC	PGA
EPROM	M2716	2K × 8-Bit	tCE = 250	X		
	M2732A	4K × 8-Bit	tCE = 250–450	X		
	M2764A	8K × 8-Bit	tCE = 250–350	X	X	
	M27128A	16K × 8-Bit	tCE = 150–300	X		
	M27256	32K × 8-Bit	tCE = 170–350	X	X	
	M27512	64K × 8-Bit	tCE = 250–350	X		
	M27011	128K × 8-Bit	tCE = 200	X		
	M27210	64K × 16-Bit	tCE = 200	X		
	M27C64	8K × 8 CHMOS	tCE = 200–350	X	X	
	M27C256	32K × 8 CHMOS	tCE = 200–250	X	X	
	J27256	32K × 8 M38510/224	tCE = 250	X		
E <sup>2</sup> PROM	M2817A	2K × 8-Bit	tCE = 250–350	X		
	M2864A	8K × 8-Bit	tCE = 250–350	X	X	
	M28256	32K × 8-Bit	tCE = 250	X		
SRAM	M2114A-4	1K × 4-Bit	tAA = 200–250	X		
	J2147H	4K × 1-Bit	tAA = 85	X		
		M38510/23801 BVX	tAA = 85	X		
		M38510/23803 BVX	tAA = 70	X		
		M38510/23805 BVX	tAA = 55	X		
		M38510/23807 BVX	tAA = 45	X		
	M2147H	4K × 1-Bit	tAA = 45–70	X		
	J2148H	1K × 4-Bit	tAA = 70	X		
		M38510/23806 BVX				
	M2148H	1K × 4-Bit	tAA = 55–70	X		
EPLD	M51C67	16K × 1-Bit CHMOS	tAA = 35–55	X		
	M51C68	4K × 4-Bit CHMOS	tAA = 35–70	X		
	M51C98	16K × 4-Bit CHMOS	tAA = 45–55	X		
	M5C060	600 Gate Erasable Program Logic	tCE = 45–55	X		
	M5C180	1800 Gate	tCE = 45–55			X

## EXPRESS (EXTENDED RELIABILITY)

EXPRESS is a service program that allows users of Intel IC components to tailor the products' electrical test flow to their specific application requirements. The test flows are designed to suit a broad range of system and production requirements.

The EXPRESS program offers users of Intel microcomputers, RAMs, EPROMs, and peripheral component families, products that are screened to operate within two industry-standard temperature ranges, each with the option of  $168 \pm 8$  hours of dynamic burn-in (equivalent to MIL-STD-883B, Method 1015). All Intel processing technologies are included. New products will enter the program as they become available.

The key to using EXPRESS is the generic matrix. You can, by specifying a two-letter prefix, select the test flow your product requires including its operating temperature range and package type. The two operating temperature ranges are: Commercial ( $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ ) and Extended ( $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ). Products are available in both hermetic ceramic and molded plastic packages, that meet these temperature specifications. Adding the option of burn-in creates the versatile EXPRESS matrix.

Temperature Range	Burn-In Hours	
	(None)	( $168 \pm 8$ )
Commercial $0^{\circ}\text{C}$ to $70^{\circ}\text{C}$	Standard	Q
Extended $-40^{\circ}\text{C}$ to $85^{\circ}\text{C}$	T	L

### EXPRESS Prefix Definitions

Standard	High Quality Standard Products
Q	Standard product with burn-in and 100% unit post burn-in electrical screening to COMMERCIAL temperature range
T	Standard product with EXTENDED temperature screening
L	Standard product with burn-in and 100% unit post burn-in electrical screening to EXTENDED temperature range

The EXPRESS test flow first subjects 100% of all products to a stringent class electrical examination. Complete DC, AC and functional parameters are tested at operating guard band temperature(s) for compliance to published specifications. Then, at your option, the product undergoes  $168 \pm 8$  hours of dynamic burn-in at  $125^{\circ}\text{C}$ . Post burn-in screening features a 100% unit electrical retest of DC, AC and functional parameters to guarantee the product's performance over its designated operating temperature range.

Both these product flows, independent of package type, then receive sample screening for electrical and visual parameters by Final Quality Assurance to 0.1% AQL. These standards are periodically reviewed, and tightened according to Intel's Corporate quality goals.

**Table 37. EXPRESS Products**

Type	Product	Description	Q	T	L
Embedded Controller	8031AH	8-Bit Single Chip Computer, without ROM, Boolean Processor, 128 × 8-Bit RAM	X	X	X
	8032AH	8-Bit Single Chip Computer, without ROM, Boolean Processor, 256 × 8-Bit RAM	X	X	X
	8035AHL	8-Bit Single Chip Computer, without ROM, 64 × 8-Bit RAM	X	X	X
	8039AHL	8-Bit Single Chip Computer, without ROM, 128 × 8-Bit RAM	X	X	X
	8040AHL	8-Bit Single Chip Computer, without ROM, 256 × 8-Bit RAM	X	X	X
	8048AH	8-Bit Single Chip Computer, 1K × 8-Bit ROM, 64 × 8-Bit RAM	X	X	X
	8049AH	8-Bit Single Chip Computer, 2K × 8-Bit ROM, 128 × 8-Bit RAM	X	X	X
	8050AH	8-Bit Single Chip Computer, 4K × 8-Bit ROM, 256 × 8-Bit RAM	X	X	X
	8051AH	8-Bit Single Chip Computer, 4K × 8-Bit ROM, 128 × 8-Bit RAM, Boolean Processor	X	X	X
	8052AH	8-Bit Single Chip Computer, 8K × 8-Bit ROM, Boolean Processor, 256 × 8-Bit RAM	X	X	X
	8085AH	8-Bit HMOS CPU	X	X	X
	80186	Highly Integrated 16-Bit CPU	X	X	
	80188	Highly Integrated 8-Bit CPU with 16-Bit Internal Architecture	X	X	
	8748H	8-Bit Single Chip Computer, 1K × 8-Bit EPROM, 64 × 8-Bit RAM	X	X	X
	8749H	8-Bit Single Chip Computer, 2K × 8-Bit EPROM, 128 × 8-Bit RAM	X	X	X
	8243	I/O Expander for Embedded Controllers	X	X	X
Microprocessor	8086	16-Bit HMOS CPU	X	X	X
	8087	Numeric Data Processor	X	X	X
	8088	8-Bit HMOS CPU, 16-Bit Internal Architecture	X	X	X
	8089	8 × 16-Bit I/O Processor	X	X	X
	80286	High Performance, Multitasking 16-Bit CPU	X		
	80287	High Performance Numeric Data Processor	X		
Support Product	8282	Parallel Bus Latch	X	X	X
	8283	Parallel Bus Latch	X	X	X
	8284A	Clock Generator for 8086, 8088	X	X	X
	82284	Clock Generator for 80286	X		
	8286	Parallel Bus Transceiver	X	X	X
	8287	Parallel Bus Transceiver	X	X	X
	8288	Bus Controller for 8086, 8088	X	X	X
	82288	Bus Controller for 80286	X		
	8289	Bus Arbiter for 8086, 8088	X		
	8755A	2K × 8-Bit EPROM with I/O Ports	X	X	X
Controller	8237A	High Performance Programmable DMA Controller	X		
	8257	Programmable DMA Controller	X		
	8259A	Programmable Interrupt-Controller	X	X	X

**Table 37. EXPRESS Products (Continued)**

Type	Product	Description	Q	T	L
Peripheral	8042	Universal Peripheral Interface 8-Bit Microcomputer			X
	8044	High Performance 8-Bit Microcontroller with 4 KBytes of On-Chip ROM	X	X	X
	8155H	256 × 8-Bit RAM, I/O Ports, Counter	X	X	X
	8156H	256 × 8-Bit RAM, I/O Ports, Counter	X		
	8203	64K Dram Controller	X		
	8251A	Programmable Communication Interface	X	X	X
	8253	Programmable Interval Timer, 3 MHz	X	X	X
	8254	Programmable Interval Timer, 8 MHz	X	X	X
	8255A	Programmable Peripheral Interface	X	X	X
	8272A	Single/Double Density Floppy Disk Controller	X		
	8274	Multi-Protocol Serial Controller	X		
	8279	Programmable Keyboard/Display Interface	X		
	8291A	GPIO Talker/Listener	X		
	8292	GPIO Controller	X		
	8293	GPIO Transceiver	X		
	8344	High Performance 8-Bit Microcontroller with On-Chip Serial Communication Processor	X	X	X
	8741A	Universal Peripheral Interface, 64 × 8-Bit RAM	X		
	8742	Universal Programmable Interface, 128 × 8-Bit RAM	X		
EPROM	2732A	4K × 8-Bit	X	X	X
	2764A	8K × 8-Bit	X	X	X
	27128	16K × 8-Bit	X	X	X
	27256	32K × 8-Bit	X	X	X
	27512	64K × 8-Bit	X	X	X
	27513	4 × 16K × 8-Bit	X	X	X
	27C64	8K × 8-Bit	X	X	X
	87C64	8K × 8-Bit	X	X	X
	27C256	32K × 8-Bit	X	X	X
	87C256	32K × 8-Bit	X	X	X
E <sup>2</sup> PROM	2817A	2K × 8-Bit	X	X	X
	2864A	8K × 8-Bit	X	X	X
NVRAM	2001	128 × 8-Bit	X	X	X
	2004	512 × 8-Bit	X	X	X
Static RAM	2114A	1K × 4-Bit, Three State	X	X	X
	2115A	1K × 1-Bit, Open Collector	X		
	2125A	1K × 1-Bit, Three State	X		
	2147H	4K × 1-Bit, Three State	X	X	X
	2148H	1K × 4-Bit, Three State	X	X	X
	2149H	1K × 4-Bit, Three State	X		



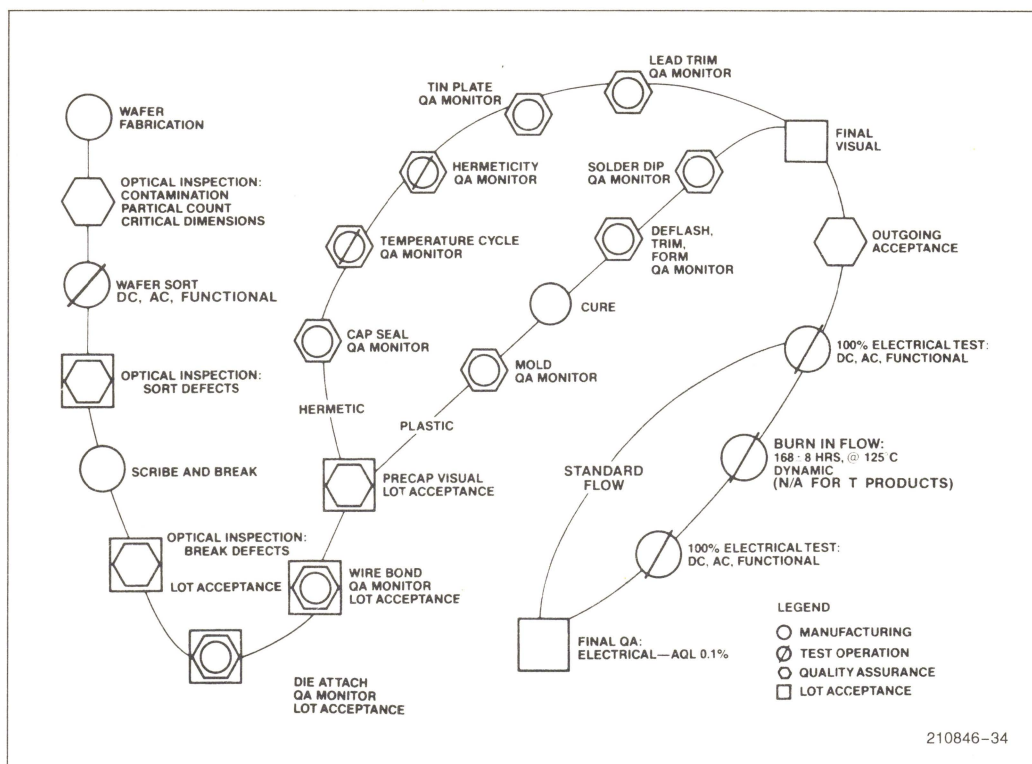


Figure 29. EXPRESS Product Manufacturing Flows

## APPLICATION SPECIFIC INTEGRATED CIRCUITS (ASIC)

One of the most important recent developments in the semiconductor industry has been the emergence of application specific integrated circuits (ASIC) as a significant factor in the marketplace. While the first two decades have been dominated by standard, mass produced chips, ASICs—custom developed for specific users and systems—are increasingly seen as a preferred alternative.

### Integrated Design Environment (IDE)

The Integrated Design Environment from Intel brings a number of unprecedented capabilities to the ASIC market. IDE includes all the products, design services and manufacturing expertise required to design and produce a complete line of ASIC products. Intel has equal strengths in all three major ASIC technologies—programmable logic, gate array, and cell-based integrated circuits.

Intel's ASIC CAE tools comprise a selection of the best the industry has to offer. Supported by a range of industry-standard hardware platforms, the ASIC libraries are available for use at Intel ASIC design centers, or at customer sites, running on customer owned host computers or workstations. Intels programmable logic, gate array and cell-based libraries feature compatible front-end design for easy transition from one ASIC product to another.

### Erasable Programmable Logic Devices (EPLDs)

The H-Series family of EPLDs contains six members ranging in complexity from 300 to 1800 gates. EPLDs are manufactured as unprogrammed CHMOS large scale integration logic devices that a user customizes through programming on a logic development system. The iPLDS (Intel Programmable Logic Development System) provides all the tools needed for creating a logic design, optimizing and custom-fitting the design to a particular EPLD device, and then programming and verifying the EPLD.

### Gate Array Integrated Circuits

Intel's ASIC products include two families of high performance gate arrays, based on Intel's 1.5 micron dual-level metal CHMOS III process and ranging in complexity from roughly 2500 to 19000 equivalent gates. One family consists of conventional gate arrays, while the second is a composite array family featuring user-definable RAM configurations and more diverse functionality.

### Cell-Based Integrated Circuits

Cell-based ICs are designed using a comprehensive library of pre-designed, fully characterized cells providing logic, memory, input/output and special functions. In addition, the library includes the cell version of the 80C51 microcontroller—and the cell equivalents of Intel microprocessor peripheral functions. The cell library is also based on Intel's 1.5 micron dual-level metal CHMOS III process.

## CELL-BASED INTEGRATED CIRCUITS

The Integrated Design Environment (IDE) design system is a flexible framework for the development, design and production of Intel ASIC products, including advanced cell-based integrated circuits. The IDE CHMOS III Cell Library is a comprehensive set of pre-designed, fully-characterized functions for the integration of system logic into high-performance, cost-effective semi-custom devices. These cells offer full-custom performance and density. The basic cell library contains logic, memory, I/O and special function cells. Also available are VLSiCELS such as the 80C51BH 8-bit microcontroller, and cell equivalents of Intel microprocessor peripheral functions. The library runs on several industry standard CAE platforms, including IBM, DEC, and EWS from Daisy Systems and Mentor Graphics. Intel cell-based ICs are produced using the same advanced, proven process used to produce Intel standard products, and are delivered with the same assurance of high quality and reliability.

### Product Highlights

#### HIGH PERFORMANCE

- 0.7 ns typical gate delay for 2-input NAND, fanout of 2
- 65 MHz D flip-flop toggle rate

#### VLSiCEL FUNCTIONS

Function	Cell Name
High-performance 8-bit microcontroller .....	80C51BH
8086 Clock Generator .....	82C84
8086 Bus Controller .....	82C88
80286 Clock Generator .....	82C84
80286 Bus Controller .....	82C88
DMA Controller .....	82C37A
Programmable Interval Timer .....	82C54
Programmable Peripheral Interface .....	82C55
Programmable Interrupt Controller .....	82C59A

#### SPECIAL FUNCTION CELLS

- RAM in standard configurations or compliant for user-defined configurations
- ROM, PLA, UART, crystal oscillator

#### TELESCOPING CELLS

- Efficient n-bit registers, counters and latches
- Minimum silicon area for “repetitive” function cells

#### I/O CELLS

- CMOS and TTL compatible
- High latch-up immunity,  $\pm 300$  ma

#### COMPATIBILITY WITH OTHER ASIC PRODUCTS

- Functionally compatible with the IDE CHMOS III Gate Array Macrocell Library

## GATE ARRAYS

Intel's VLSI experience coupled with an established gate array capability gives system designers a bridge between standard architectures and semi-custom solutions. Access to this gate array capability is through Intel's Integrated Design Environment (IDE), a comprehensive set of CAD tools and symbol and simulation model libraries for the development, design, and production of Intel ASIC products. The libraries are supported by popular CAD tools, including Engineering Workstations from Daisy Systems and Mentor Graphics, IBM and DEC. Intel's initial gate array offerings are its D15A gate array and D15C composite array series, both based on Intel's CHMOS III 1.5 micron dual-layer metal technology. The D15A series features an extensive library of macrocells. The D15C series features the same macrocell library plus special functions implemented efficiently by all-level personalization of the base wafer. The first special function to be included in the D15C series is RAM. Planned additions to the library include Intel 8086 and 80286 peripheral functions.

### Product Highlights

- More than 100 unique macrocells in the library, expanding to include LSI and VLSI peripheral functions
- Functionally compatible with the IDE CHMOS III Cell Library for designing cell-based integrated circuits.
- 0.7 ns typical gate delay for 2-input NAND, fanout of 2; 65 MHz typical D flip-flop toggle rate
- High-density 1.5 micron, dual-layer metal CHMOS III process
- Proven CAD tools allow high block\* utilization
- Optional support for Level Sensitive Scan Design (LSSD) featuring automatic test generation
- Flexible options for on-chip RAM
- Selectable performance-level options for SSI and MSI macrocells, expanding total number of available macrocells
- Full line of industry-standard packages
- Controlled Collapsed Chip Connection (C4) bonding option provides increased I/O capability

**Table 38. Intel Gate Arrays—1.5 Micron Technology**

Gate Arrays				
Device	Equivalent Gates*	Blocks	Max I/O Pins	Min Power Pins
D15A020	2,550	2,000	62	6
D15A040	5,100	4,000	78	6
D15A065	8,287	6,500	112	10
D15A066	8,410	6,600	103	9
D15A070	9,017	7,072	137	9
D15A098	12,495	9,800	112**	10**
D15A100	12,750	10,000	174	9
D15A150	19,125	15,000	174**	9**
Composite Arrays—2304 Bits Configurable RAM				
D15C001	6,196	4,860	103	9
D15C002	10,700	8,392	174	9

\*Gate is 2-input NAND equivalent. Experience has demonstrated 1.275 gates/block with six transistors/block. Actual number of gates/block is design dependent.

\*\*Preliminary.



## **H-SERIES EPLDs (ERASABLE PROGRAMMABLE LOGIC DEVICES) AND THE iPLDS (INTEL PROGRAMMABLE LOGIC DEVELOPMENT SYSTEM)**

Intel's H-Series EPLDs consist of six devices ranging from 300 to 1800 gates. Based on reliable and flexible EPROM technology, these devices enable users to develop and mass produce a custom circuit using standard, off-the-shelf components. EPLDs are supported with an advanced set of development tools hosted on the PC. The iPLDS is an easy-to-use system for creating a logic design, optimizing and "custom-fitting" the design to a particular EPLD, and programming and verifying the device. The iPLDS development kit includes a plug-in PC card, a programming module, complete documentation including design examples, and sample EPLDs. The EPLDs are manufactured using Intel's CHMOS II-E process technology to assure systems designers high-performance, low-power devices maintaining Intel's strict commitment to the highest quality and reliability standards.

### **Product Highlights**

#### **H-SERIES CMOS EPLDs—ERASABLE PROGRAMMABLE LOGIC DEVICES**

- Low power, 50 mW typical standby power
- 300–1800 gate complexity
- 100% generic testability
- Advanced architectures; D, T, RS and JK registers; asynchronous clocks
- Programmable security bit
- High performance; 35 ns combinatorial device speeds, 30 MHz clock rates

#### **iPLDS—INTEL PROGRAMMABLE LOGIC DEVELOPMENT SYSTEM**

- Includes software, programmable hardware, and sample EPLDs
- Low Cost
- Able to minimize and compile designs for complex, 1800-gate EPLDs
- Interfaces to PC-based schematic entry tools; DASH-2™\* (FutureNet), PC-CAPSTM\*\* (P-CAD)
- Generates output in standard JEDEC file format

\*DASH-2™ is a trademark of FutureNet.

\*\*PC-CAPSTM is a trademark of P-CAD

## DESIGN SERVICES

The Intel Integrated Design Environment (IDE) provides a flexible system for developing, designing, and producing EPLD, gate array and cell-based integrated circuits. The system includes complete CAE tool suites as well as symbol libraries and simulation models hosted on a variety of industry-standard CAE platforms. The IDE is supported by an expanding group of design centers providing training classes, expert local technical support, and access to Intel mainframes. Designs executed using the IDE are produced using advanced Intel process technology and proven manufacturing capability, with strict adherence to Intel quality and reliability standards.

## Product Highlights

### DESIGN CENTERS AND REGIONAL APPLICATIONS SPECIALISTS

- Local resources for training, library support, design analysis and consultation
- Access to Intel IDE hardware and software

### LIBRARIES AVAILABLE ON A VARIETY OF CAE PLATFORMS

- CIEDS\* Environment: IBM PC AT and IBM RT PC, and IBM 30XX and 43XX mainframes
- SDS/LOGIX-SL\*\* Environment; DEC VAX\*\*\* 11/7XX, 86XX, MicroVax and Vaxstation
- Daisy Environment: all workstations from Daisy Systems
- Mentor Graphics Environment: all workstations from Mentor Graphics

### LEADERSHIP VERIFICATION TOOLS

- Physical layout and design verification tools combine the best of commercially available hardware and software with more than two decades of Intel design expertise

### PROVEN MANUFACTURING CAPABILITY

- 1.5 micron CHMOS III process for high performance and high density
- Same process used for Intel standard components

### SUPERIOR QUALITY AND RELIABILITY LEVELS

- Complete gate array and cell-based qualification program covers process, libraries and packages—assuring exceptional quality and dependable performance to specifications
- Special requirements can be accommodated

## Semi-Custom Design Methodology

Customers typically complete all design steps through simulation and timing verification, then transfer the design to Intel. At that point, the customer and Intel agree on a Design Specification which will serve as a benchmark throughout manufacturing, assembly and final test.

# SINGLE BOARD COMPUTERS

## MULTIBUS® BOARDS

The components that make the ‘Open System’ a reality . . . It all begins with MULTIBUS® System Architecture: the industry standard architecture. The foundation of Intel’s microcomputer systems architecture was laid in 1976 with the introduction of the MULTIBUS system bus, and Intel’s first single board computer product, the iSBC® 80/10 board. It was a solution the microcomputer industry needed to make microprocessor technology easier to use and more readily available for new product design and development. Its widespread use and popularity made it a defacto industry and IEEE standard (IEEE 796).

The bus architecture is the conceptual foundation and physical framework for interfacing the various pieces of the microcomputer system into a family of system solutions. This family now includes single board computers, memory expansion boards, a broad array of I/O expansion products, packaging products, microsystem software and integrated microsystems.

Support for multiple levels of expansion and design flexibility.

The five levels of iSBC expansion supported by Intel’s MULTIBUS provide OEMs with the widest range of cost/performance solutions and open system flexibility in the industry.

- The MULTIBUS System Bus—system communication and interconnection
- The iLBX Execution Bus—large amounts of high speed memory
- The MULTICHANNEL™ I/O Bus—very high speed, high performance I/O
- The iSBX I/O Expansion Bus—low cost modular I/O
- iSBC MULTIMODULE Add-ons—on-board memory and math expansion
- BITBUSTM Distributed Control Bus—fast serial connection to microcontroller

Intel continues to develop new iSBC products to meet the industry’s need for powerful, cost-effective, single board computer products. There are now more than 65 MULTIBUS expansion boards. There are also over 250 MULTIBUS vendors providing more than 2500 MULTIBUS compatible products, the largest assortment of compatible products in the industry today.

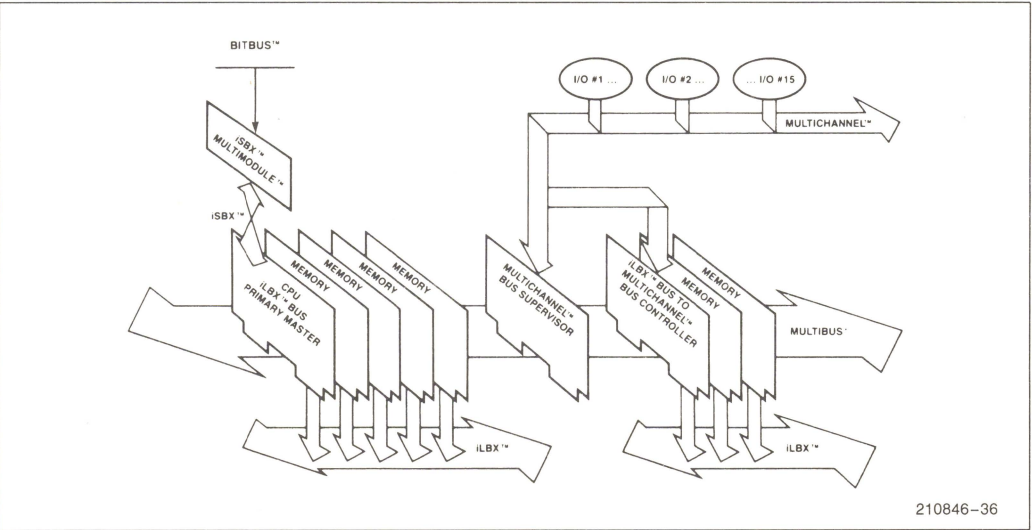


Figure 30. Distributed Control Modules

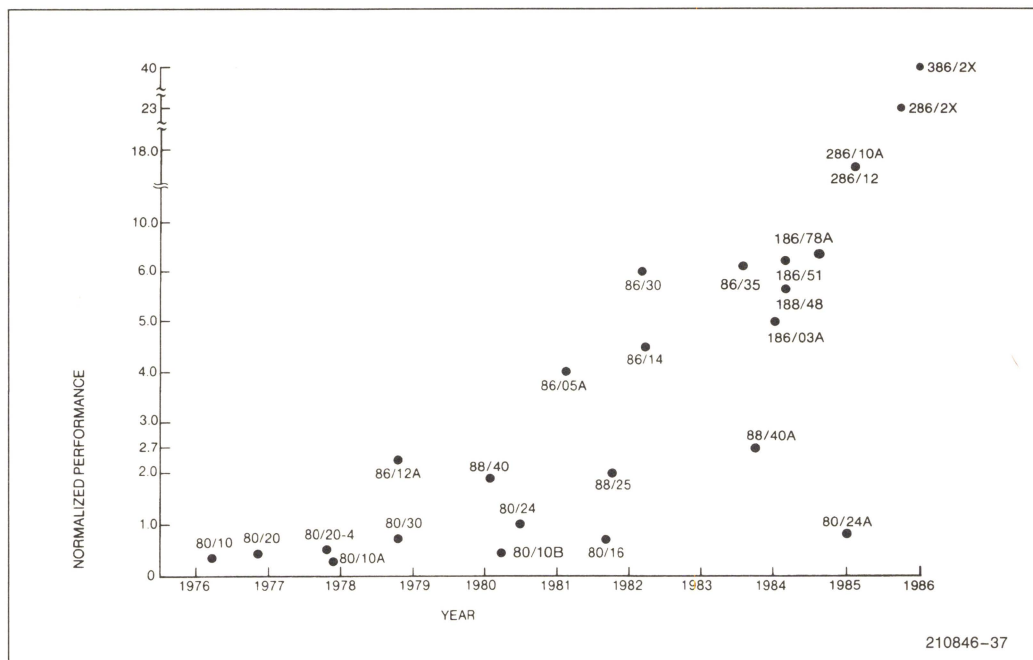


Figure 31. iSBC® CPU Boards—Relative Performance

Table 39. MULTIMODULE™ Expansion Options

MULTIMODULE™ BOARDS		iSBC® Boards																		
Expansion	Product	286/ 10A	286/ 12	86/ 05A	86/ 12A	86/ 14	86/ 30	86/ 35	186/ 03A	186/ 51	186/ 78A	88/ 25	88/ 40A	88/ 45	80/ 10B	80/ 20-4	80/ 24A	80/ 30	286/ 2X	386/ 2X
RAM EPROM	iSBC® 341	■	■	■					■		■	■	■	■					■	■
RAM EPROM	iSBC® 340				■															
H.S. Math	iSBC® 337A			■	■	■	■	■				■	■	■						
512K RAM	iSBC® 314							■												
128K RAM	iSBC® 304						■	■		■										
8K RAM	iSBC® 302			■								■								
4K RAM	iSBC® 301												■							
32K RAM	iSBC® 300A					■														
32K RAM	iSBC® 300				■															
Bubble Memory	iSBX™ 258	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■		
1 MB DRAM																			■	■
2 MB DRAM																			■	■
4 MB DRAM																			■	■
8 MB DRAM																			■	■



**Table 40. MULTIBUS® CPU Boards**

Product	CPU(1)	RAM	EPROM E <sup>2</sup> PROM	iSBXTM(2) Expansion Connectors	MULTIMODULETM(2) Expansion	Operating(3) System Software
iSBC 286/10A	80286	0–128 Kb	0–512 Kb	2	iSBC 341	iRMX 86 iRMX 286 XENIX+ 286 CP/M* 286
iSBC 286/12	80286	1 Mb	0–256K	2	iSBC 341	
iSBC 186/51	80186 82586	128 Kb	6,28-pin JEDEC sites	2	iSBC 304	iNA 960 iRMX 86
iSBC 186/03A	80186	0-64 Kb	0–512 Kb	2	iSBC 341	iRMX 86
iSBC 188/48	80188	64 Kb	2, 28-pin JEDEC sites	2	iSBC 341, iSBC 307	iRMX 86
iSBC 86/30	8086-2	128 Kb	8–64 Kb	2	iSBC 304 iSBC 337/A	iRMX 86 CP/M 86
iSBC 86/14	8086-2	32 Kb	8–64 Kb	2	iSBC 300A iSBC 337/A	iRMX 86 CP/M 86
iSBC 86/12A	8086	32 Kb	4–16 Kb	0	iSBC 300 iSBC 340 iSBC 337/A	iRMX 86 CP/M 86
iSBC 86/05A	8086-2	8Kb	8–16 Kb 8–256 Kb	2	iSBC 302 iSBC 341 iSBC 337/A	iRMX 86 CP/M 86
iSBC 88/45	8088 (8/16-bit)	16K	64K–128K	2	iSBC 341	iRMX 86 CP/M 86
iSBC 88/40A	8088 (8/16-bit)	4 Kb	16–32 Kb	3	iSBC 301 iSBC 341 iSBC 337/A	iRMX 86
iSBC 88/25	8088 (8/16-bit)	4 Kb	4–64 Kb	2	iSBC 302 iSBC 341 iSBC 337/A	iRMX 86 CP/M86
iSBC 80/30	8085A (8-bit)	16 Kb	8–8 Kb	0	iSBC 304	CP/M 80
iSBC 80/24A	8085A (8-bit)	8K	4–32 Kb	2	iSBC 301	CP/M 80
iSBC 80/20-4	8080A (8-bit)	4K	4–8 Kb	0	—	CP/M 80
iSBC 80/10B	8080A	1K-4K	4–16 Kb	1	—	—
iSBC 86/35	8086-2	512 Kb	32–256 Kb	2	iSBC 304 iSBC 314 iSBC 337/A	iRMX 86
iSBC 186/78A	80186 82720	512 Kb	8, 28-pin	2	iSBC 343 iSBC 341	iVDI 720
286/2X	80286	1–8 MB	384K	1	MMOX	iRMX, XENIX
386/2X	80386	1–16 MB	512K	1	MMOX	iRMX XENIX, UNIX* V

**NOTES:**

1. See Microprocessor Section.

2. See following tables.

3. See Software Section.

\*CP/M is a trademark of Digital Research, Inc.

+ XENIX is a trademark of Microsoft Corp.

\*UNIX is a trademark of Bell Laboratories.

**Table 41. MULTIBUS® Memory Expansion Boards**

Product	Memory Type	Memory Size (Bytes)	Parity	iLBX™ Interface	High Speed Interface
iSBC 28A	Dynamic RAM	128K	Yes	No	No
iSBC 056A	Dynamic RAM	256K	Yes	No	No
iSBC 012B	Dynamic RAM	512K	Yes	No	No
iSBC 012C	Dynamic RAM	512K	Yes	No	No
iSBC 010CX	Dynamic RAM	1M	Yes	Yes	No
iSBC 020CX	Dynamic RAM	2M	Yes	Yes	No
iSBC 012CX	Dynamic RAM	512K	Yes	Yes	No
iSBC 012EX	Dynamic RAM	512K	Yes	Yes	Yes
iSBC 010EX	Dynamic RAM	1M	Yes	Yes	Yes
iSBC 020EX	Dynamic RAM	2M	Yes	Yes	Yes
iSBC 040EX	Dynamic RAM	4M	Yes	Yes	Yes
iSBC 428	28-Pin Universal Site	0–1M	No	Yes	No
iSBC 300	Dynamic RAM	32K	No	No	No
iSBC 300A	Dynamic RAM	32K	No	No	No
iSBC 301	Static RAM	4K	No	No	No
iSBC 302	Static RAM	8K	No	No	No
iSBC 304	Dynamic RAM	128K	No	No	No
iSBC 340	24 Pin EPROM	4 Jedec Sites	No	No	No
iSBC 341	24/28 Pin EPROM/RAM	4 Jedec Sites	No	No	No
iSBC 254	Bubble Memory	128K–512K	Yes (Auto)	No	No
iSBX 251	Bubble Memory	128K	Yes (Auto)	No	No
iBCK 10	Bubble Memory Cassette	128K	Yes (Auto)	No	No
iBCK 12	Bubble Proto Cassette	128K	Yes (Auto)	No	No
MM01	DRAM	1 MB	Yes	No	No
MM02	DRAM	2 MB	Yes	No	No
MM04	DRAM	4 MB	Yes	No	No
MM08	DRAM	8 MB	Yes	No	No

**Table 42. MULTIBUS® Memory and I/O Expansion Boards**

Product	RAM	EPROM	Serial I/O	Parallel I/O	
				Lines	Connectors
iSBC 108A	8K	4-32K	1 (RS232C)	48	2
iSBC 116A	16K	4-32K	1 (RS232C)	48	2

**Table 43. MULTIBUS® Analog I/O Expansion Boards**

Product	Input Channels	Output Channels	MULTIMODULE™ Type
iSBX 311	8–16		iSBX Single Wide
iSBX 328		8	iSBX Single Wide

**Table 44. MULTIBUS® Digital Interface and I/O Expansion Boards**

Product	Description	I/O Capacity	Type
iSBC 569	Intelligent 8085-driven Digital I/O Slave	48 I/O Lines	MULTIBUS
iSBC 519	General Purpose Digital I/O	72 I/O Lines	MULTIBUS
iSBC 556	Optically-Isolated Digital I/O	48 I/O Lines	MULTIBUS
iSBC 350	Programmable I/O iSBX MULTIMODULE	24 I/O Lines	Single-Wide iSBX MULTIMODULE
iSBX 488	IEEE 488 GPIB/HPIB	16 I/O Lines 16 Control	Single-Wide iSBX MULTIMODULE
iSBX 351	Programmable serial I/O MULTIMODULE Board	1—I/O Port RS232C or RS422	Single-Wide iSBX MULTIMODULE
iSBC 589	Intelligent Multichannel DMA Controller	8/16-bit 1—MULTICHANNEL Port 2—iSBX Connectors	MULTIBUS
iSBC 580	MULTICHANNEL Bus to iLBX Bus Interface	1—16-bit MULTICHANNEL 1—16-bit iLBX Interface	MULTIBUS
iSBX 352	Programmable Serial I/O Module	1—I/O Port RS232C or RS422 SDLC/HDLC Only	Single Wide iSBX MULTIMODULE
iSBX 354	Programmable Serial I/O Module	2—I/O Ports RS232C or RS422	Single Wide iSBX MULTIMODULE

**Table 45. MULTIBUS® High Speed Math Boards**

	Chip	Speed	Fixed	Floating	Transcendental	
iSBX 331	8231	4 MHz	Yes	Yes	Yes	
iSBC 337	Execution Time (Microseconds)		Multiply	Divide	Add	Subtract
		Fixed	28	48	20	20
		Floating Point	29	40	29	37
iSBC 337A	Execution Time (Microseconds)	Fixed Floating Point	12 13	20 16	8 12	8 15

**Table 46. Mass Storage Controllers**

Product	No. of Boards	Interface Supported Transfer Rates	No. of Drives Supported	S/W Support
iSBC 208	1	SA800/850; SA400/450/460 8" –62.5 KBytes/sec 5¼" –31.25 KBytes/sec	4	iRMX 86
iSBC 215G	1	ANSI X3T9/1226 (1 Mbyte/sec transfer rate) in burst mode	4	iRMX 86 XENIX
iSBC 215G Kit (includes external data separator)	2	ST506/412 (transfer rate 5 Mbits/sec)	4	iRMX 86 XENIX
iSBX 217C	Single wide MULTIMODULE	QIC-02 or 3M HCD-75 (90K, 30K, 17K - depending on tape drive speed)	4	iRMX 86 XENIX
iSBX 218A	Double wide MULTIMODULE	SA800/850; SA400/450/460 5¼" –31.25 KBytes/sec 8" –62.5 KBytes/sec	4	iRMX 86 XENIX iRMX 286
iSBC 220	1	SMD (transfer rate 10 Mbits/sec)	4	iRMX 86
iSBC 226	1	Enhanced SMD (transfer rate 15 Mbits/sec)	2	iRMX 86
iSBC 186/03A	1	SCSI-single host environment (transfer rate 1.2 Mbytes/sec asynchronous)	single target environment	iRMX 86
iSBC 214	1	ST 506/412 (5 Mbits/sec)	2	RMX 86
		SA 450/460 (31.25 KBytes/sec)	4	RMX 286
		QIC-02 (90K, 30K, 17K, Depending on Tape Drive and Speed)	4	XENIX

**Table 47. MULTIBUS® Human Interface**

Product	Display Resolution	Character Size	Color or B.W.	Frame Rate
iSBX 270	80 Characters 24/80 24 Lines	5 × 7, 7 × 9 6 × 8	8 color or B&W	50 Hz or 60 Hz
iSBX 275	512 × 512 × 1 256 × 256 × 3	Up to 8 × 8	8 color or B&W	50 Hz or 60 Hz
iSBC 186/78A	640 × 480 × 4 1024 × 768 × 1	N/A	16 color or 16 Grey	50 Hz or 60 Hz



## MULTIBUS® II ARCHITECTURE

Anticipating the demand for a bus with advanced features, Intel announced the MULTIBUS II architecture specification in November 1983. Requirements ranging from handling high performance 32-bit microprocessor CPU boards through increasing system performance and bandwidth through multi-processing are addressed by the MULTIBUS II bus architecture specification. Coupled with this demand for increasingly higher performance are other factors determined to be equally critical in developing advanced technology systems. These other factors include more and faster memory and I/O capabilities, highly reliable systems with high data integrity, flexible software with real-time applications, and systems that are easy to use and improved methods for sharing system information, resources, and processing.

MULTIBUS II bus is an open architecture suitable for a wide range of processor-independent applications. The multiple bus architecture includes three bus structures that are compatible with two existing MULTIBUS I I/O buses. The three new MULTIBUS II bus structures are the Parallel System Bus (iPSB), a 32-bit bus with 40M byte/sec throughput, the Local Bus Extension (iLBX II) offering high speed (48M byte/sec) access to large amounts of off-board memory, and the Serial System Bus (iSSB), a low cost serial interconnect offering the flexibility of MULTIBUS II boards being physically extended up to 10 meters apart. Carried over from the MULTIBUS I architecture are the iSBX™ I/O Expansion Bus and the MULTICHANNEL DMA (Direct Memory Access) I/O Bus. Choices can be made between implementation of any or all of the five buses depending on what functionality is to be optimized, a philosophy known as “functional partitioning”.

An additional strength of MULTIBUS II rests with the definition of a standard bus interface. Intel has implemented this bus interface definition using VLSI technology and thus provides the key to multi-processing with intelligent boards that are processor-independent. The Message Passing Coprocessor (MPC) is a semicustom VLSI device that minimizes the real estate required for full bus interface, maximizes bus performance, increases reliability, lowers costs and increases design flexibility. The MPC offloads the local on-board CPU by handling all bus arbitration and the message space interface, eliminating the interface bottleneck present in traditional shared memory.

Individually, the buses represent significant advances in bus architecture design. Together, they represent an evolutionary path to future VLSI technology, compatibility, and flexibility.

## MULTIBUS® II PRODUCTS

Intel's family of MULTIBUS II products allow users to take immediate advantage of the bus advances outlined in the MULTIBUS II Architecture Specification. Using the building blocks offered by Intel in the open MULTIBUS II bus architecture provides the flexibility and ease of use demanded by either today's high performance applications or tomorrow's technology driven markets.

**Table 48. MULTIBUS® II Single Board Computer CPU Products**

Product	Description
iSBC 386/100 Single Board Computer	<ul style="list-style-type: none"> <li>• 16 MHz 32-Bit 80386 Microprocessor</li> <li>• MULTIBUS II iPSB interface for multimaster configurations and multiprocessing system expansion</li> <li>• High speed 64K Byte static RAM cache on-board providing zero-wait state memory reads</li> <li>• 80287 Numeric Data Co-Processor</li> <li>• Four DMA channels supplied by the 82258 Advanced DMA controller with 8 Mbytes/sec transfer rate</li> <li>• MULTIBUS II interconnect space for software configurability and diagnostics</li> <li>• Resident firmware to support Built-In-Self-Test (BIST) at power up and power fail recovery</li> <li>• 1, 2, 4 or 8 Mbytes of on-board dual-ported dynamic RAM memory with parity error detection; expandable to 16 Mbytes</li> <li>• 8- or 16-bit iSBX bus (IEEE P959) interface with DMA for I/O expansion</li> <li>• One RS 232C serial I/O port</li> <li>• Double-high Eurocard standard form factor, pin and socket DIN connectors</li> </ul>
iSBC 286/100A Single Board Computer	<ul style="list-style-type: none"> <li>• 8 MHz 80286 Microprocessor</li> <li>• MULTIBUS II iPSB interface for multimaster configurations and multiprocessing system expansion</li> <li>• MULTIBUS II iLBX II (Local Bus Extension) interface for high-speed memory expansion</li> <li>• MULTIBUS II interconnect space for software configurability and diagnostics</li> <li>• Resident firmware to support Built-In Self-Test (BIST) power-up diagnostics</li> <li>• Optional 80287 Numeric Data Co-Processor (socket on-board)</li> <li>• Two iSBX bus interface connectors for I/O expansion bus</li> <li>• Four DMA channels supplied by the 82258 Advanced DMA controller with 8 Mbytes/sec transfer rate</li> <li>• 16 levels of vectored interrupt control and up to 255 distinct interrupt sources and 255 interrupt destinations are supported using message-based interrupts</li> <li>• Two 28-pin JEDEC sites</li> <li>• 24 programmable I/O lines configurable as SCSI interface, Centronics interface, or general purpose I/O</li> <li>• Two programmable serial interfaces, one RS 232C, the other RS 232C or RS 422A compatible</li> <li>• Double-high Eurocard standard form factor, pin and socket DIN connectors</li> </ul>
iSBC 186/100 Single Board Computer	<ul style="list-style-type: none"> <li>• 8 MHz 80186 Embedded Controller</li> <li>• MULTIBUS II iPSB interface for multimaster configurations and multiprocessing system expansion</li> <li>• Two programmable serial interfaces, one RS232C DTE and the other RS422 DTE</li> <li>• One parallel port configurable for SCSI, Centronics, or General Purpose</li> <li>• Socket for full iSBX compatibility and BITBUS support</li> <li>• 512 KByte Dual Port DRAM supported on iPSB</li> <li>• 8 MHz Advanced Direct Memory Access Controller (ADMA) plug in option</li> <li>• MULTIBUS II interconnect space fully supported with 8751 controller</li> <li>• Double high Eurocard standard form factor, pin and socket DIN connectors</li> </ul>

**Table 49. MULTIBUS® II Memory Products**

Product	Description
iSBC MEM/312 Cache-Based MULTIBUS II RAM Board	<ul style="list-style-type: none"> <li>• 512 KByte Dual Port RAM board</li> <li>• High-speed cache-based boards with 8 KBytes of cache RAM</li> <li>• 32-bit MULTIBUS II Parallel System Bus (iPSB) and Local Bus Extension (iLBX II) interface support</li> <li>• Zero wait state over iLBX II on a cache hit, one wait state for cache misses, and writes at 8 MHz</li> <li>• Double-high Eurocard standard form factor, pin and socket DIN connectors</li> <li>• MULTIBUS II software interconnect support for dynamic memory configuration and diagnostics with no jumpers necessary on the board</li> <li>• Built-In-Self-Test (BIST) diagnostics on-board with both LED indicators and software access to error information</li> <li>• Automatic memory initialization at power-up and at power-fail recovery</li> <li>• Byte-parity error detection</li> </ul>
iSBC MEM/310 Cache-Based MULTIBUS II RAM Board	<ul style="list-style-type: none"> <li>• 1M Byte Dual Port RAM board</li> <li>• High-speed cache-based boards with 8 KBytes of cache RAM</li> <li>• 32-bit MULTIBUS II Parallel System Bus (iPSB) and Local Bus Extension (iLBX II) interface support</li> <li>• Zero wait state over iLBX II on a cache hit, one wait state for cache misses, and writes at 8 MHz</li> <li>• Double-high Eurocard standard form factor, pin and socket DIN connectors</li> <li>• MULTIBUS II software interconnect support for dynamic memory configuration and diagnostics with no jumpers necessary on the board</li> <li>• Built-In-Self-Test (BIST) diagnostics on-board with both LED indicators and software access to error information</li> <li>• Automatic memory initialization at power-up and at power-fail recovery</li> <li>• Byte-parity error detection</li> </ul>
iSBC MEM/320 Cache-Based MULTIBUS II RAM Board	<ul style="list-style-type: none"> <li>• 2M Byte Dual Port RAM board</li> <li>• High-speed cache-based boards with 8 KBytes of cache RAM</li> <li>• 32-bit MULTIBUS II Parallel System Bus (iPSB) and Local Bus Extension (iLBX II) interface support</li> <li>• Zero wait state over iLBX II on a cache hit, one wait state for cache misses, and writes at 8 MHz</li> <li>• Double-high Eurocard standard form factor, pin and socket DIN connectors</li> <li>• MULTIBUS II software interconnect support for dynamic memory configuration and diagnostics with no jumpers necessary on the board</li> <li>• Built-In-Self-Test (BIST) diagnostics on-board with both LED indicators and software access to error information</li> <li>• Automatic memory initialization at power-up and at power-fail recovery</li> <li>• Byte-parity error detection</li> </ul>

**Table 49. MULTIBUS® II Memory Products (Continued)**

Product	Description
iSBC MEM/340 Cache-Based MULTIBUS II RAM Board	<ul style="list-style-type: none"> <li>• 4M Byte Dual Port RAM board</li> <li>• High-speed cache-based boards with 8 KBytes of cache RAM</li> <li>• 32-bit MULTIBUS II Parallel System Bus (iPSB) and Local Bus Extension (iLBX II) interface support</li> <li>• Zero wait state over iLBX II on a cache hit, one wait state for cache misses, and writes at 8 MHz</li> <li>• Double-high Eurocard standard form factor, pin and socket DIN connectors</li> <li>• MULTIBUS II software interconnect support for dynamic memory configuration and diagnostics with no jumpers necessary on the board</li> <li>• Built-In-Self-Test (BIST) diagnostics on-board with both LED indicators and software access to error information</li> <li>• Automatic memory initialization at power-up and at power-fail recovery</li> <li>• Byte-parity error detection</li> </ul>
iSBC MEM/601 Universal Site MULTIBUS II Memory Board	<ul style="list-style-type: none"> <li>• Two banks of eight 28-pin JEDEC sockets</li> <li>• ROM and EPROM up to 64K × 8</li> <li>• EEPROM, SRAM, and iRAM up to 32K × 8</li> <li>• 512 × 8 NVRAM</li> <li>• Full iLBX II and iPSB support</li> <li>• Data retention after power fail with optional lithium battery back-up on-board</li> </ul>

**Table 50. MULTIBUS® II Communication Products**

Product	Description
iSBC 186/410 Serial Communications Computer	<ul style="list-style-type: none"> <li>• 8 MHz 80186 Embedded Controller</li> <li>• Six serial communication channels, expandable to 10 channels via iSBX bus connectors</li> <li>• Four DMA channels supplied by the 82258 Advanced DMA controller with 8 Mbytes/sec transfer rate</li> <li>• Supports RS 232C only on 4 channels; RS 422A or RS 232C interface configurable on 2 channels</li> <li>• 256 Kbytes DRAM provided, expandable to 512K bytes DRAM on board</li> <li>• MULTIBUS II Interconnect space for software configurability and diagnostics</li> <li>• Resident firmware to support Built-In Self-Test (BIST) at power-up and power fail recovery</li> <li>• Four 28-pin JEDEC memory sites</li> <li>• Two iSBX connectors for I/O expansion</li> <li>• Double high Eurocard standard form factor, pin and socket DIN connectors</li> </ul>
iSBC 186/530 Ethernet (IEEE 802.3) Communications Engine	<ul style="list-style-type: none"> <li>• 8 MHz 80186 Embedded Controller</li> <li>• 82586 Local Area Network Coprocessor for Ethernet (IEEE 802.3) compatible networking capability</li> <li>• 256 Kbytes DRAM provided, expandable to 512K bytes DRAM on board</li> <li>• MULTIBUS II Interconnect space for software configurability and diagnostics</li> <li>• Resident firmware to support Built-In Self-Test (BIST) at power-up and power fail recovery</li> <li>• MULTIBUS II iPSB Interface for multimaster configurations and multiprocessing system expansion</li> <li>• Four 28-pin JEDEC memory sites</li> <li>• One serial debug port</li> </ul>



**Table 51. MULTIBUS® II Support Products**

Product	Description
iSBC CSM/001 Central Services Module	<ul style="list-style-type: none"> <li>Integrates MULTIBUS II central system functions on a single board</li> <li>MULTIBUS II Parallel System Bus (iPSB) clock generation for all agents interfaced to the MULTIBUS II iPSB bus</li> <li>System-wide reset signals for power-up, warm start, and power failure/recovery</li> <li>System-wide time-out detection and error generation</li> <li>Slot I.D. and Arbitration I.D. initialization</li> <li>MULTIBUS II interconnect space for software configurability and diagnostics</li> <li>Built-In-Self-Test (BIST) power-up diagnostics with LED indicator and error reporting accessible to software via interconnect space</li> <li>General purpose link interface to other standard (MULTIBUS I) or proprietary buses</li> <li>Time-of-day clock support with battery back-up on board</li> <li>Double-high Eurocard standard form factor, pin and socket DIN connectors</li> </ul>
iSBC LNK/001 MULTIBUS II to MULTIBUS I Link Board	<ul style="list-style-type: none"> <li>Dual port 128 KByte DRAM programmable via MULTIBUS II interconnect space</li> <li>Supports 16- and 24-bit address and 8- and 16-bit data paths</li> <li>16M Bytes of MULTIBUS I memory maps into MULTIBUS II memory space</li> <li>32 KBytes of MULTIBUS I/O memory maps into MULTIBUS II I/O memory space</li> <li>Converts MULTIBUS I interrupts into MULTIBUS II interrupt messages</li> <li>MULTIBUS I form factor board connecting to iSBC CSM/001 via flat ribbon cable</li> </ul>

**Table 52. MULTIBUS® II Test Products**

Product	Description
MB II GPTF General Purpose Tester—Functional	<ul style="list-style-type: none"> <li>Functional tester for testing MULTIBUS II boards in a systems environment</li> <li>Tests up to four MULTIBUS II boards simultaneously in a range from ambient temperature to 70°C</li> <li>Voltage and temperature margins are software controlled</li> <li>Multiprocessor, multitesting functional tester with totally automated test sequence requires minimum human interface</li> <li>Powerful command language for troubleshooting and evaluation</li> <li>One free STBL (System Test Board Level) test is included. Additional test programs are available for Intel MULTIBUS II boards</li> <li>Video monitor for error message display and test status</li> <li>Bus drawer feature on P2 connector allows user flexibility to test boards with different types of P2 interfaces</li> <li>Safety features including thermal cut out at 90°C</li> <li>Available in either USA, Japan or International power configuration</li> </ul>

**Table 53. MULTIBUS® II Software Products**

Product	Description
iRMX 86 Operating System Release 7	<ul style="list-style-type: none"> <li>• MULTIBUS II support for iSBC 286/100 is a configuration option applications in Real Address Mode, including support for the SCSI peripheral interface and up to 1M Byte addressability</li> <li>• Interprocessor signal support</li> <li>• Automatic software configuration of memory boards</li> <li>• Support for battery backed-up, global time of day clock</li> <li>• Extendable to allow addition of custom device drivers</li> </ul>
iSDM 286 80286 System Debug Monitor	<ul style="list-style-type: none"> <li>• Development support for iSBC 286- and 80286 based applications</li> <li>• Real Address Mode (RAM) and Protected Virtual Address Mode (PVAM) support</li> <li>• Support of MULTIBUS I and MULTIBUS II environments</li> <li>• Powerful debugging commands, including single step CPU operation</li> <li>• Software configuration of MULTIBUS II system boards at start-up and automatic configuration of memory boards</li> <li>• Universal Development Interface (UDI) support via development system connection</li> <li>• Command execution, including program load capability from Intellec Series III or Series IV Development systems</li> <li>• Supports 80287 Numeric Processor Extension (NPX) for high speed math applications</li> </ul>

**Table 54. MULTIBUS® II Packaging Products**

Product	Description
iSBC PKG/606 and iSBC PKG/609 MULTIBUS II Card- cage Assemblies	<ul style="list-style-type: none"> <li>• Available in two sizes to hold up to six or nine MULTIBUS II boards</li> <li>• Designed to mount inside a chassis or other enclosure</li> <li>• Uses a 6 layer Parallel System Bus (iPSB) backplane</li> <li>• All lines fully terminated per the iPSB MULTIBUS II specification</li> <li>• Assembly uses aluminum extrusion construction for strength and rigidity</li> <li>• Accommodates Intel iSBC PKG/902 and iSBC PKG/903 2 and 3 slot iLBX II backplanes</li> </ul>
iSBC PKG/902 and iSBC PKG/903 MULTIBUS II iLBX II Backplanes	<ul style="list-style-type: none"> <li>• Provides iLBX II interconnect for fastest CPU and off-board data memory transfers</li> <li>• Designed to mount in MULTIBUS II cardcage assemblies</li> <li>• Available in 2 slot (iSBC PKG/902) and 3 slot (iSBC PKG/903) sizes</li> <li>• Uses a fully terminated six layer backplane</li> <li>• Includes a 10 pin connector for BITBUS applications</li> <li>• Meets all electrical and mechanical requirements of the MULTIBUS II specification</li> </ul>
iSBC PKG/622 MULTIBUS II Front Panels	<ul style="list-style-type: none"> <li>• Front panels for attaching to custom MULTIBUS II boards, mounting iSBX MULTIMODULES, or filling empty slots in MULTIBUS II systems</li> <li>• Full adherence to MULTIBUS II specification with "U" shaped extruded aluminum to meet EMI/RFI requirements</li> <li>• Kit contains front panels, ejector tabs, and all mounting hardware</li> </ul>
SYP/500 MULTIBUS II System Chassis	<ul style="list-style-type: none"> <li>• Full enclosure MULTIBUS II design development tool</li> <li>• 3 full height 5.25" peripheral bays</li> <li>• 6 slot MULTIBUS II cardcage assembly</li> <li>• 3 slot iLBX II backplane</li> <li>• 270 watt power supply</li> </ul>

**Table 55. MULTIBUS® II System Products**

Product	Description
SYP MB2 MULTIBUS II Starter System	<ul style="list-style-type: none"> <li>• Ready to run MULTIBUS II system based on Intel's 80286 microprocessor with optional 80287 numeric coprocessor</li> <li>• Supports industry standard iRMX Operating System and languages</li> <li>• 1M Byte RAM on iSBC MEM/310</li> <li>• 320 KByte floppy</li> <li>• 40M Byte Winchester</li> </ul>

**Table 56. MULTIBUS® II Peripheral Controller Products**

Product	Description
iSBC 186/224 MULTIBUS II Peripheral Controller Board	<ul style="list-style-type: none"> <li>• High performance peripheral controller with 80186 embedded controller, 128 KByte DRAM, track caching, and DMA</li> <li>• Winchester interface supports up to 4 ST506/412, 5¼" drives, on board diagnostics, and ECC</li> <li>• Tape interface supports up to 4 QIC-02 streaming tape drives</li> <li>• Floppy interface supports up to 4 5¼" floppy drives, single or double sided, single or double density</li> <li>• Peripheral Communication Interface (PCI) gives command queuing capability</li> <li>• Real-time multi-tasking Operating System</li> </ul>

**Table 57. MULTIBUS® II Compatible iSBX™ MULTIMODULES**

Product	Description
iSBX 331	• High speed math board for fixed and floating point math
iSBX 258	• Interface MULTIMODULE board for Intel bubble cassette system
iSBX 350	• Parallel digital I/O MULTIMODULE board
iSBX 351	• Serial Communication MULTIMODULE board
iSBX 352	• SDLC/HDLC serial Communication MULTIMODULE board
iSBX 354	• Dual channel serial digital I/O MULTIMODULE board
iSBX 488	• General Purpose Interface Bus (GPIB) MULTIMODULE board
iSBX 311	• Analog input MULTIMODULE board
iSBX 328	• Analog output MULTIMODULE board
iSBX 344	• BITBUS distributed control bus MULTIMODULE Board

**NOTE:**

All MULTIMODULE boards are fully functional with the MULTIBUS II product line. This listing indicates which MULTIMODULE boards will attach directly to the CPU board without requiring any additional cabling.



## PERSONAL COMPUTER ENHANCEMENT PRODUCTS

Intel's Personal Computer Enhancement Operation (PCEO) offers a variety of add-in products for IBM PCs and compatibles through retail distribution channels. The product line includes memory expansion and multifunction boards, and math coprocessors.

### INTEL'S ABOVE™ BOARD FAMILY

Above Boards topple the 640K conventional memory barrier imposed by DOS 3.X, increasing the personal computer's memory capacity to 8 Mbytes above the previous 640K limit. Four models are available; all are supported by a variety of major software packages.

All Above Boards feature menu-driven installation, RAM disks, a print buffer, and diagnostic software. In addition, all boards are covered by a five-year warranty.

The Above Board/PC and the Above Board PS/PC provide conventional and expanded memory on a single board. The Above Board AT and the Above Board PS/AT provide extended (protected mode) memory in addition to conventional and expanded memory.

#### ABOVE BOARD/PC

The Above Board/PC is used to fill out conventional memory and add up to 2 Mbytes of expanded memory in an IBM PC, XT, or compatible.

#### ABOVE BOARD PS/PC

The Above Board PS/PC is the new standard in multifunction cards for PCs, XTs, and compatibles. It has a parallel and a serial port, clock/calendar with battery backup, and up to 1.5 Mbytes of memory.

#### ABOVE BOARD/AT

The Above Board/AT provides up to 2 Mbytes of conventional, expanded, and extended memory for IBM PC ATs and compatibles.

#### ABOVE BOARD PS/AT

The Above Board PS/AT provides up to 1.5 Mbytes of memory, plus a parallel and a serial port, for IBM PC ATs and compatibles.

#### ABOVE BOARD PIGGYBACK MEMORY

Up to 2 Mbytes of memory can be added with a Piggyback Memory Board to the Above Board/AT or Above Board PS/AT.



**Table 58. Above™ Board Configurations**

Model Number	Product	Maximum Total Memory
<b>For the IBM PC, XT and compatibles:</b>		
PCMB1010	Above Board/PC with 64K*	512K
PCMB1020	Above Board/PC with 256K*	2 MB
PCMB1110	Above Board PS/PC with 64K*	384K
PCMB1120	Above Board PS/PC with 256K*	1.5 MB
<b>For the IBM AT and compatibles:</b>		
PCMB2010	Above Board/AT with 128K** With Piggyback Memory Board	1.6 MB 3.6 MB
PCMB2020	Above Board/AT with 512K** With Piggyback Memory Board	2 MB 4 MB
PCMB2110	Above Board PS/AT with 128K** With Piggyback Memory Board	384 KB 996 KB
PCMB2120	Above Board PS/AT with 512K** With Piggyback Memory Board	1.5 MB 3.5 MB

**NOTES:**

\*These boards can be configured with up to 384K of conventional memory, with the remainder available as expanded memory. Above Board/PC and Above Board PS/PC are compatible with the IBM PC, XT, PC Portable, COMPAG Portable, COMPAG Deskpro, AT&T 6300, and Zenith Z-100.

\*\*These boards can be configured with up to 128K of conventional memory, with the remainder available as expanded and/or extended memory. Above Board/AT and Above Board PS/AT are compatible with the IBM PC/AT, COMPAG Portable 286, and COMPAG Deskpro 286.

## 8087/80287 MATH COPROCESSOR FAMILY

Intel's Math Coprocessors can dramatically boost your PC's performance by speeding math-intensive calculations (including spreadsheets and graphics). Math Coprocessors work with hundreds of major personal computer software packages, and they are quick and easy to install. The following table matches Math Coprocessors to computers.

**Table 59**

Coprocessor	System and Speed of System
8087	For 5 MHz IBM PC, XT, and compatibles.
8087-2	For 8 MHz IBM PC, and compatibles.
80287	For 6 and 8 MHz IBM PC ATs, compatibles, and accelerator boards.
80287-8	For IBM PC AT, and compatibles and accelerator boards operating faster than 8 MHz.

## OEM SYSTEMS

Intel's microcomputer systems are the result of Intel's experience and leadership in the design and manufacturing of advanced microprocessors and single board computers. Combine these with continued advances in VLSI technology in areas such as graphics and communications and further advances in software capabilities, Intel now offers very powerful, yet flexible microcomputer systems for OEM, VARs, and end-users.

Intel's microcomputer systems consist of the System 300 series of microcomputer systems family of products. Enhanced system features are provided through Intel's OpenNet Family of single board communications products and the iNA 960, XENIX-Net, and iRMX-Net Networking Software.

### SYSTEM 300 SERIES SUPERMICROS

#### System 300 Series—Three High-Performance Microsystem Solutions

The Intel family of System 300 microcomputers consists of three high-speed multiuser systems, offering a broad continuum of expansion options and price/performance advantages.

The first member of the System 300 family is Intel's System 310 microcomputer. At the heart of the System 310 is the industry's leading microprocessor; the Intel 6 MHz 80286 processor, which delivers more than twice the performance of previous generations of 16-bit microprocessors. The 80287 numeric coprocessor assists in providing unmatched throughput for numeric-based applications.

The second System 300 configuration is Intel's System 310 AP (Advanced Processor), which uses the more powerful 8 MHz 80286 microprocessor. According to benchmark studies, the 8 MHz 80286 central processor offers up to 80 percent improved performance over other systems, including Intel's 6 MHz 80286 processor. The most powerful XENIX-based, single-CPU microsystem on the market, the System 310 AP supports up to 16 users and is available with three integrated peripherals—floppy and Winchester disk drives and streaming cartridge tape.

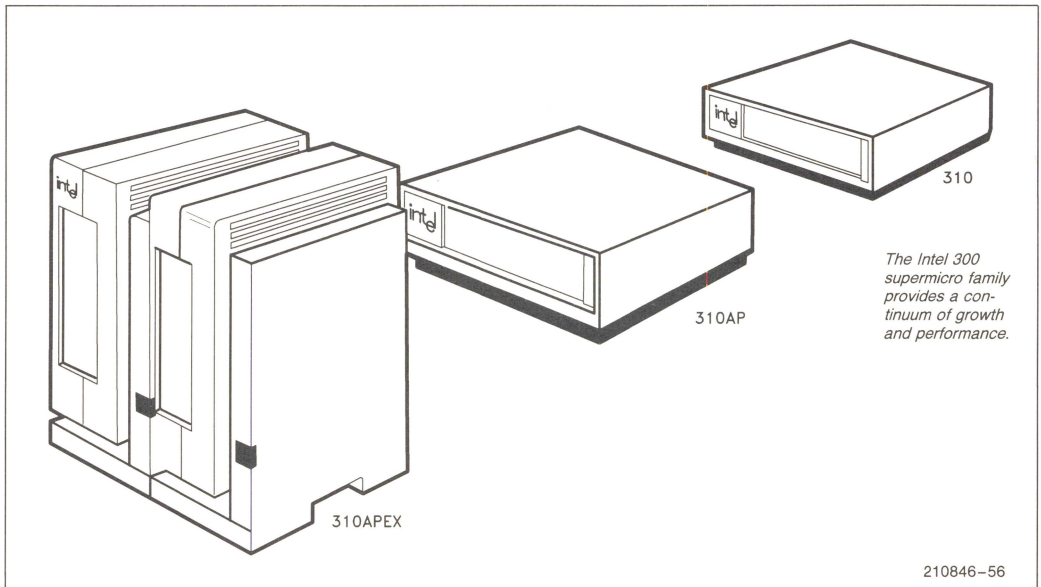


Figure 32. Intel System 300 Series

The third member of Intel's supermicro family is the System 310 APEX (Advanced Processor Extension), which is based on the simple concept that two or more processors are better than one. Designed around the 8 MHz 80286 microprocessor, the System 310 APEX is offered in dual-, triple- and even quadruple-processor configurations.

While Intel's multiple-CPU architecture is transparent to the XENIX application, it can boost system performance by as much as 1.7 times with each additional CPU. In fact, the System 310 APEX CPU performance is clocked at five millions-of-instructions-per-second (MIPS), or five times that of Digital Equipment Corporation's VAX 11/780 minicomputer.

## OPEN SYSTEM ARCHITECTURE—BUILDING ON STANDARDS

The Intel System 300 Series is an outgrowth of Intel's commitment to the Open System design concept. Virtually every System 300 Series component—microprocessors, buses, interfaces, peripherals, and operating system software—is a product of industry standards. Intel's commitment to using industry standards allows its microsystems to evolve and keep pace with changes in technology.

Through Open System architecture, Intel protects its customers' long-term investment in hardware and XENIX software applications. For example, System 310s can be upgraded easily to System 310 APs, which in turn can become higher-performance APEX systems simply by adding up to three processors.

Intel's modular approach to microcomputer systems is a cost-effective alternative to acquiring additional minicomputers or even a mainframe. As the number of system users increases and as commercial application become more data-intensive, additional processors and mass storage peripherals can be added. In short, as a user's needs grow, so do Intel's systems.

## Expandable for Future Application and Performance Needs

Designing the System 300 Series around an Open Systems foundation using MULTIBUS guarantees system compatibility and expandability. As a result, Intel microsystems are never obsolete. To date, Intel's industry leadership in standardizing the MULTIBUS bus design (IEEE 796) has resulted in 170 vendors with over 1,200 available add-in board level products for System 300 Series expansion.

Intel supermicro configurations provide between zero and six MULTIBUS board slots for expansion and customization, depending on the base configuration. The expansion possibilities are as varied as each user's needs. Disk controllers, communications boards, graphics interfaces, memory expansion, and many other specialized single-board computer products are available for configuring special system applications.

**Table 60. System 300 Series Configurations**

System Number of Users	310 AP-17 2	310 AP-44 4	310 AP-41 8	310 AP-42 8	310 AP-88 8	310 AP-142 8	310 AP-82 12	310 AP-141 Server*	310 AP-143 12	310 AP-145 Server*	310 AP-146 16
Microprocessor	80286 8 MHz	80286 8 MHz	80286 8 MHz	80286 8 MHz	80286 8 MHz	80286 8 MHz	80286 8 MHz	80286 8 MHz	80286 8 MHz	80286 8 MHz	80286 8 MHz
Numeric Coprocessor	80287	80287	80287	80287	80287	80287	80287	80287	80287	80287	80287
RAM Memory Expandable to	1 MB 9 MB	1 MB 9 MB	1 MB 9 MB	1 MB 9 MB	2 MB 9 MB	2 MB 9 MB	2 MB 9 MB	1 MB 9 MB	2 MB 9 MB	2 MB 9 MB	2 MB 9 MB
Mass Storage (unformatted)	19 MB Win- chester	40 MB Win- chester	40 MB Win- chester	40 MB Win- chester	85 MB Win- chester	140 MB Win- chester	85 MB Win- chester	140 MB Win- chester	140 MB Win- chester	140 MB Win- chester	140 MB Win- chester
Serial I/O Ports Expandable to	2 18	6 18	10 18	10 18	10 18	10 18	14 18	2 18	14 18	10 18	18 18
Tape Backup	NA	NA	NA	60 MB	60 MB	60 MB	60 MB	60 MB	60 MB	60 MB	60 MB
Parallel Ports	1	1	1	1	1	1	1	1	1	1	1

### NOTE:

\*Server delivered with OpenNET controller integrated (SXM552).



## Increasing Storage Capacity— The 311 Peripheral Expansion Solution

The 311 peripheral expansion subsystem is Intel's solution for applications that require greater storage and archival backup capabilities. A member of the System 300 product family, the 311 comes with three full-height 5¼ inch bays that provide a full range of peripheral expansion options, including Winchester disk drives and streaming cartridge tape.

Users requiring greater Winchester disk storage capacities than those provided by the System 300 system unit now have the option of adding three full-height 5¼ inch Winchester disk drives. The 311 can be configured with a choice of 40 MB, 85 MB, or 140 MB drives, providing a maximum of 660 MB disk storage.

The 5¼ inch streaming tape option supports the user with 60 MB of back-up capacity. Thus, a 40 MB Winchester disk drive can be quickly and reliably backed up with a single tape cartridge. The tape option provides a convenient method of removable archiving, since one tape cartridge can replace more than 100 floppy diskettes.

The 311 expansion subsystem is open to many combinations of 5¼ inch peripherals. It can be arranged in a configuration with two full-height Winchester drives and tape, or in many other configurations, such as tape only. As a complete storage expansion solution, Intel provides all external cables, power supplies, controller boards, and documentation required to connect the 311 to a System 300 host.

## SPEECH TRANSACTION PRODUCTS

The Intel Speech Transaction Family, iSBC 570, iSBC 576 and iSBC 577, is a set of products that provides a minimal risk path to adding speech Input/Output (I/O) to your product line. The Speech Transaction Family will allow you to move from evaluation to integral speech driven products without major redesigns. Depending on your stage of product development, whether it is an evaluation, a product simulation, an add-on speech option, or a fully integrated speech product, the Speech Transaction Family's flexibility allows your speech I/O application to grow with a minimal amount of engineering effort.

The iSBC 570, Speech Transaction Development Set will plug directly into your RMX86 based SYS310 System. The iSBC 576, Speech Transaction Board is compatible with Intel MULTIBUS single board computers, peripherals, card cages, and power supplies. If you desire, the iSBC 576 can be used with any non-MULTIBUS host system by communication via a RS232C serial link.

**Table 61. Speech Transaction Products**

Product	Description
iSBC 570 (Speech Transaction Development Set)	Complete Development Support Set for Intel Speech Product Family. The set includes: <ul style="list-style-type: none"> <li>• Speech Transaction Generator</li> <li>• iSBC 576 Speech Transaction Board</li> <li>• iSBC 575 Operator Control Unit</li> <li>• Microphone</li> <li>• Demo Program</li> </ul> This package is intended to provide the ability for technology evaluation, application development and application simulation.
iSBC 576 (Speech Transaction Board)	The iSBC 576 Speech Transaction Board is the heart of a speech I/O system. Besides providing Automatic Speech Recognition (ASR), a ROM-resident Speech Transaction Manager is included on the board. This provides a flexible operating structure for the system designer with a fully buffered speech generated input—transaction handling capability.



## MICROCOMMUNICATIONS SYSTEMS

Intel's MultiSERVER™ and FASTPATH™ provide a comprehensive array of network features/services and the ability to connect Intel microcomputer systems to IBM System 370 mainframes.

### MultiSERVER™

In addition to Intel's OpenNet Product Family, Intel also provides OpenNet users the added features and benefits of the OpenNet MultiSERVER and related services. MultiSERVER includes a host of network services and features including:

- XENIX Operating System with enhanced ease of use, added drivers.
- Async/Bisync Communication Subsystem including
  - 3270 Bisync, Hasp, and 2780/3780 RJE Emulation
  - 3277/3278 Display and Printer Emulation
  - Async Terminal Services, Modem Access and Serial Printer Connect
- SNA Emulation Gateway Subsystem featuring
  - 3274 SNA Cluster Emulation
  - 3278/3287 Display and Printer Emulation
- iBASE, Application and Administration Software Environment

Intel's OpenNET MultiSERVER provides the OpenNET user a comprehensive, multiple service, high performance server for integrating PCs and other information systems including File, Print, Communication, Network Application and Administration services.

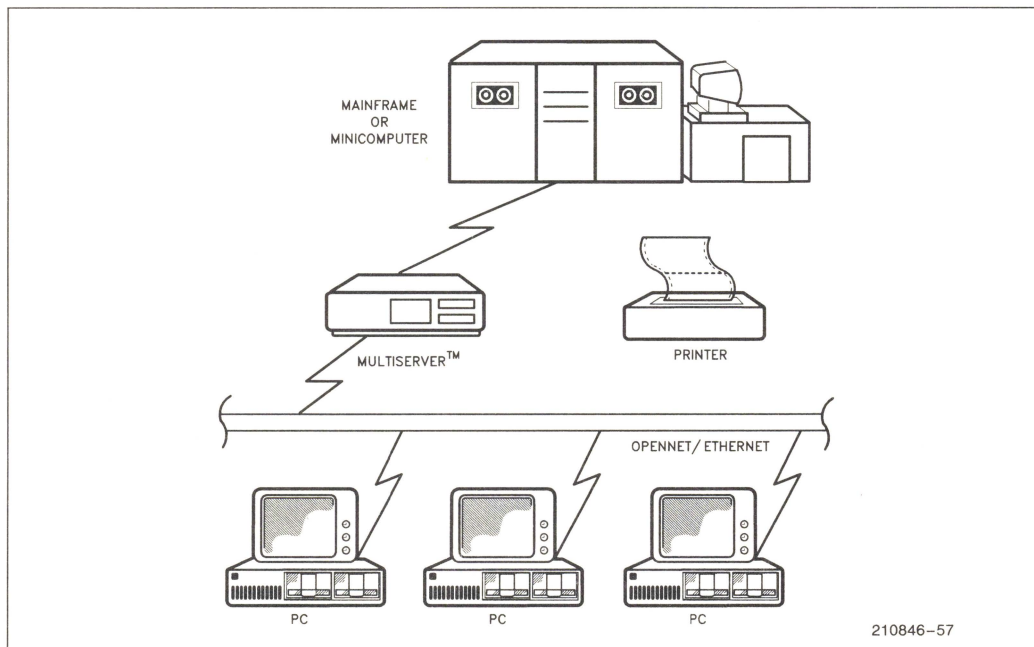


Figure 33. Typical MultiSERVER™ Environment

## Multiple Services

**File Services:** File services for our integrated department service network have been optimized for easy sharing of data and programs. Transparent network file access lets the user work with files anywhere on the network as if they are resident on his/her PC—without having to transfer files from one network location to another.

And to ensure that all files are safely archived, and to enhance control and administration, MultiSERVER features centralized, cost-effective tape back-up.

**Print Services:** OpenNET MultiSERVER maximizes the cost-effectiveness and flexibility of print resources on the department service network through shared access and print spooling.

Expensive laser and letter-quality printers, for example, can be shared among numerous users from one MultiSERVER site and need not be duplicated at each workstation.

Users can queue up multiple printing jobs as schedules dictate and check the status of these jobs.

**Network Application Services:** Intel's network application services let users harness the complete spectrum of resources available on the department service network.

With one service, VIRTUAL TERMINAL, PCs and terminals can gain access to MultiSERVERs or other computers and execute applications resident there. This service significantly extends the capability of users on the department service network by allowing them to access special shared data and applications—such as payroll or accounts payable—that are beyond the scope of a personal computer. Remote users at scattered workstations conveniently run applications with virtual terminal as if directly attached to the MultiSERVER or other computer.

REMOTE BATCH schedules activities efficiently, designating certain jobs for later execution on remote computers as suitable.

ELECTRONIC MAIL, improves communication among users on the department service network.

**Administrative Services:** An easy-to-use, human interface makes administration of your department service network a productive process. Add or delete users easily. Readily establish links to mainframes or change the status of a printer. Designate file locations. All within seconds. Our administrative services are designed to make management, security, and control of your department service network a winning proposition.

**Communication Services:** To integrate Intel MultiSERVERs, PCs, and terminals with IBM mainframes and department minicomputers, MultiSERVER emulates both IBM SNA and BISYNC protocols.

Serving as a single, central link to the mainframe, MultiSERVER can provide a cost-effective gateway for numerous PCs and terminals. MultiSERVER communications services supply access to critical mainframe data and applications, and allow users to extract and download data from a remote mainframe into a PC or departmental database for operation on that data locally.

**Network Maintenance and Support Services:** No other vendor today matches the level of service and support available with Intel's OpenNET MultiSERVER products.

Intel's network service team provides complete, broad-based support of your department service network, beginning with consultation and planning to ensure that the products you select best suit your environment and applications.

Once your Intel products arrive, to get you up and running quickly, we take responsibility for installation and thorough check-out of your department service network.

And in the months and years that follow, Intel ensures that you derive the greatest possible benefit from our products by providing a wide range of training programs, and ongoing support of software and hardware, including both Intel and non-Intel components.

## OpenNET™ MultiSERVER™

### Intel's OpenNET MultiSERVER System for Department Service Networks

The personal computer revolution has dramatically extended the boundaries of personal productivity, making data generation and analysis faster and more effective than ever before. But paradoxically, while individual productivity has soared, organizational effectiveness has lagged far behind expectations.

Solutions presented to date are largely inappropriate, disjoint or piecemeal strategies requiring individuals and organizations to devote large amounts of time and resources to connect, administer and maintain islands of computer systems—not to mention the tremendous amount of time required to manage several vendor relationships.

ENTER INTEL's OpenNET MultiSERVER solution to the organizational productivity slump. OpenNET and MultiSERVER represents the **FIRST FULLY INTEGRATED, HIGH PERFORMANCE AND EXPANDABLE DEPARTMENT SERVICE NETWORK**, linking Intel MultiSERVERs, PCs, Intel multiuser supermicrocomputer systems, terminals, mainframes, minis, peripherals, data, and applications in one seamless system.

MultiSERVER's high level of integration offers several key advantages. First, it means that we can implement your department service network immediately, providing all the necessary services and products for a complete, coordinated solution. Readily installable into an existing base of PCs, and friendly to users of all experience levels, OpenNET MultiSERVER turns group productivity around fast.

Next, because you purchase your department service network from one source, Intel, your users enjoy a consistent, integrated view of services. Instead of inefficiently and slowly learning to access different systems for each required service, your users conveniently turn to one solution for every need.

MultiSERVER's super-performance is the result of incorporating several high speed processors and high capacity storage devices into its design. This means that data and services are delivered to users **FAST**. MultiSERVER automatically distributes service tasks to highly intelligent subsystems so that PC users can concurrently access data around the network, download data from multiple mainframe computers, and print lengthy reports at multiple printing devices without having to contend for often oversaturated resources.

And with the ability to incorporate up to three additional application processing modules as needed, MultiSERVER can **GROW IN PLACE** to handle more complex services, add more PC users, or add lower cost terminal users—or all three. In fact, a single MultiSERVER can grow into a complete **DEPARTMENT COMPUTER SYSTEM** handling database and accounting applications in addition to providing a complete set of network services for a group of PCs.

### MultiSERVER™: One Server, Multiple Services

At the heart of the OpenNet department service network is the Intel System 310 AP, a MultiSERVER supermicro-computer which provides a choice of comprehensive services to PC users. MultiSERVER software boosts group productivity by making a broad range of new services available to all participants on the network—not to just pockets of users here and there.

Data and applications, as well as special resources such as mass storage, back-up devices, host communications links and high-quality printers, can be shared among users, maximizing economy and efficiency.

Intel's department service network is also convenient and easy to use. Menu-driven software guides users comfortably through the task at hand, and because the extended services emanate from Intel MultiSERVERs instead of numerous, discrete servers, users enjoy uniform services.

Finally, when you need to increase the capacity of your department service network, additional MultiSERVERs can be integrated transparently and economically—so that your department service network remains productive as you grow.

## Complete Services for an Integrated Solution

Intel's OpenNET MultiSERVER solution offers a comprehensive array of flexible network services to improve information exchange, strengthen decision-making, and increase the cost-effectiveness of networked PCs.

### FASTPATH™

FASTPATH is a Channel to MULTIBUS® Adapter connecting the Intel MULTIBUS architecture to an IBM System 370 I/O channel and other processors conforming to the 370 I/O specification.

FASTPATH acts as a high-speed interface, between the channel and a MULTIBUS-based application, achieving throughput rates of up to 3 million bytes per second.

### FASTPATH™ Features

Data Streaming transfer mode, at 3 Megabytes per second, is supported by FASTPATH on an IBM System 370 I/O interface as well as up to 3 Megabytes per second in high-speed data transfer mode.

An optional Two Channel Switch connects FASTPATH to two channels on one IBM host or one channel on each of two hosts (field installable).

An optional remote maintenance feature provides for the remote diagnosis of hardware problems.

FASTPATH's hardware consists of a Channel Adapter, a Control Processor and 6 slots for MULTIBUS-compatible application boards.

The Channel Adapter is the interface between the MULTIBUS-based application and up to two IBM channels, and supports block-multiplexer and selector type channels.

The Control Processor controls the activities of the Channel Adapter and defines the "personality" or way in which the I/O channel will be handled.

### FASTPATH™ Applications

Some typical FASTPATH applications include connecting an IBM mainframe to one or more Local Area Networks, Wide Area Networks, dissimilar hosts, special peripherals—all running your choice of protocol.

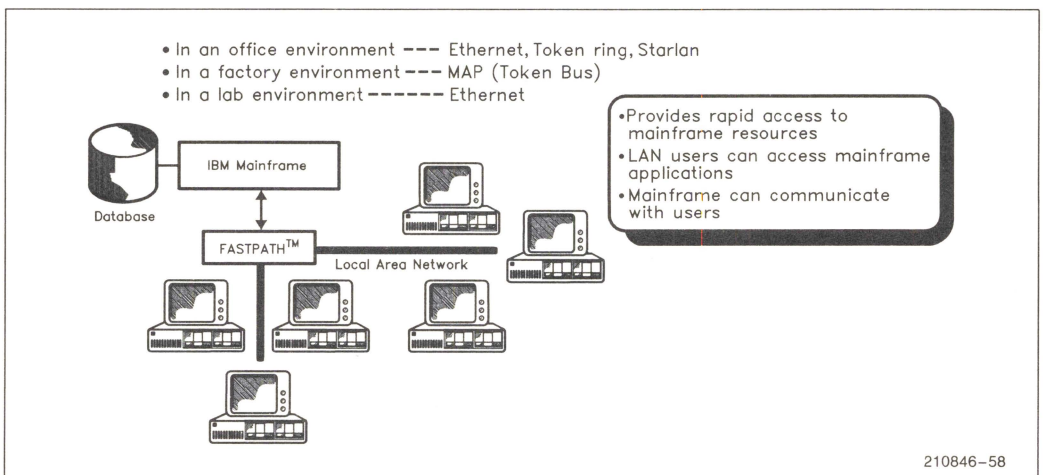
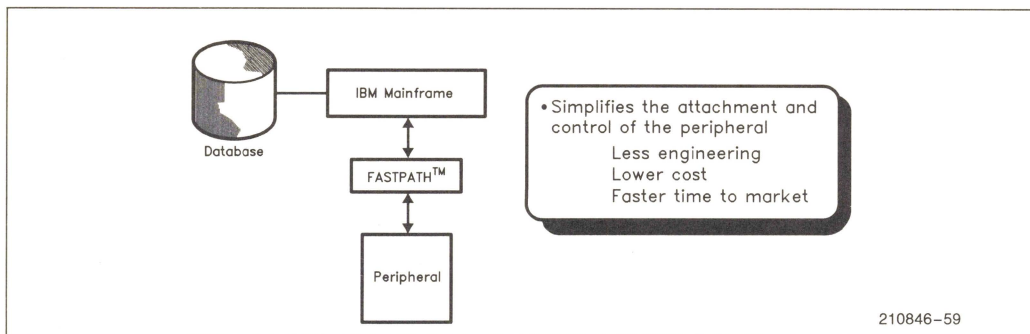


Figure 34. High Performance Connection Between a Mainframe and Local Area Networks

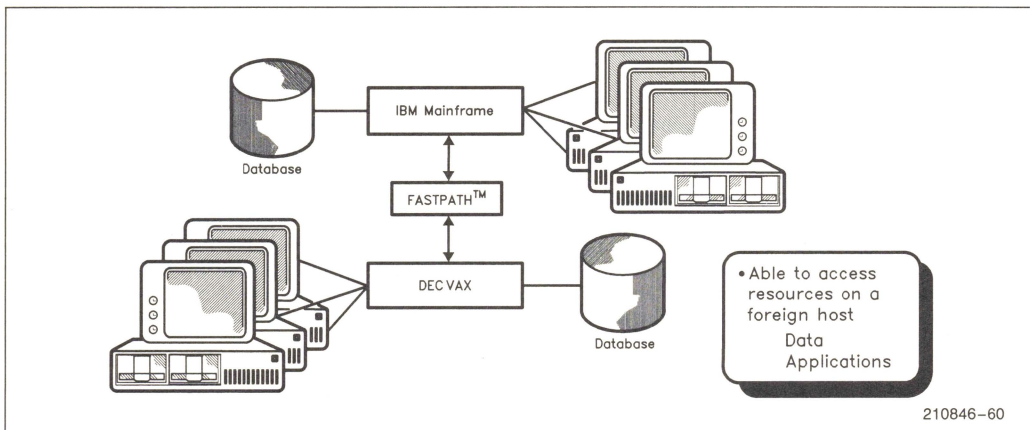




**Figure 35. Channel Connection Between a Mainframe and a Specialized Peripheral Device**

### Fastpath™ High Speed IBM to VAX Connection

The Intel 9750 FASTPATH control unit provides the complete connection for IBM System/370 class mainframes to Digital Equipment Corporation (DEC) VAX Minicomputers.



**Figure 36. Connection Between an IBM Mainframe and DEC VAX 11/7XX Minicomputers**

With FlexLINK software (from FlexLINK International Corporation) added to FASTPATH, a high speed bi-directional connection is provided for a DEC VAX or MicroVAX II and the mainframe. The FASTPATH + FlexLINK product can also act as a bridge between IBM System Network Architecture (SNA) networks and DEC-net networks.

The FASTPATH + FlexLINK product implementation allows IBM and DEC users to share high speed access to data files and initiate tasks on each other's systems.

The FASTPATH + FlexLINK product implementation transparently links IBM 43XX and 30XX class mainframes and DEC VAX and MicroVAX II systems. DEC users may access a remote IBM processor as though native to that computer using FlexLINK's full screen IBM 3278 terminal emulation capability. IBM users can similarly access the DEC processor.

FlexLINK software is compatible with the security features that each system provides.

FASTPATH + FlexLINK product features include remote peripheral access and high speed file transfer capabilities. Remote peripheral access lets users share expensive devices such as high speed laser printers. High speed file transfer eliminates the throughput constraints of communication-based links such as gateways and provides conversion between ASCII and EBCDIC data formats.

# PARALLEL SUPERCOMPUTER

## IPSC™ CONCURRENT COMPUTER

The iPSC concurrent computer is the first family of expandable concurrent computers. It is designed to be a flexible base of hardware and software upon which to build concurrent programming tools and application programs.

The iPSC system consists of one, two, or four computational units. Each unit contains up to 32 high-performance microcomputers or nodes, each with its own numeric processing unit and local memory. The microcomputers are interconnected in a hypercube topology. A resident node operating system, in conjunction with communication coprocessors, provides the user application with process-to-process message delivery capabilities, from standard Fortran, C, and LISP\* languages.

The iPSC system also includes Intel's MULTIBUS®-based System 286/310 microcomputer which is connected to each node by a shared communication channel. The System 310 serves as Cube Manager, providing the user interface to the Cube as well as hosting the programming tools and system diagnostics.

## THE IPSC-VX VECTOR CONCURRENT SUPERCOMPUTER

The iPSC™-VX system (vector extension) is a vector concurrent computer system, an enhanced member of the iPSC family. The iPSC-VX offers true supercomputer performance for the individual scientist or research team, and provides the tools for developing efficient, high-performance applications in a large-scale parallel computing environment.

The cost of owning and maintaining a conventional supercomputer has made high-end scientific computing inaccessible to all but a privileged few. The iPSC-VX system changes this. By using low cost VLSI to harness the complementary technologies of concurrent and vector processing, the iPSC-VX system sets a new price-performance standard. The result is supercomputer performance at the price of a supermini.

The iPSC-VX family builds upon the basic architecture of the iPSC concurrent computer. By coupling a high-performance vector processor to each of the iPSC processing nodes, the vector enhancement results in dramatically improved computational performance for both vector and scalar operations. Optimized to meet the mathematical requirements of scientific computation, the iPSC-VX series is ideal for such applications as circuit simulation, structural analysis, fluid dynamics, and oil reservoir modeling.

An iPSC-VX system consists of 16, 32, or 64 computational nodes. Each node consists of an independent microcomputer with its own CPU, communications control, local memory, and dedicated vector processor. In keeping with the basic iPSC architecture, the processing nodes in a system are interconnected using a hypercube topology where connected nodes are supported with reliable point-to-point message delivery service.

## CONCURRENT COMMON LISP™

Concurrent Common LISP\* (CCLISP) is an implementation of Common LISP designed to run on the Intel iPSC™ concurrent computer family. As an emerging industry standard, Common LISP provides the foundation for a broad base of AI development tools and applications. Concurrent Common LISP extends this powerful environment to allow multiple Common LISP processes to cooperate asynchronously and spawn new processes via message passing on Intel's concurrent computer architecture.

CCLISP is a complete development tool kit for the iPSC computer consisting of:

- CCLISP resident on each iPSC node with 4.5 MBytes of memory
- message passing mechanisms to implement concurrency between nodes from standard LISP constructs
- network services to link LISP workstation development, and provide remote evaluation of common LISP forms

CCLISP's Common LISP functionality is an extension of GCLISP 286 Developer™ (GCLISP v2.0), which supports the large memory (15 MByte) addressability of Intel's 82086, the 80287 math co-processor, and a compiler.

\*Concurrent Common LISP™ is a trademark of Gold Hill Computers Inc.

**Table 62. System Specifications**

System Feature	iPSC/d5	iPSC/d6	iPSC/d7
Number of Nodes	32	64	128
Number of Spare Nodes	1	2	4
Total System RAM Memory	16 MBytes (expandable)	32 MBytes (expandable)	64 MBytes
Total Node-to-Node Communication Channels	80	192	448
Cube Footprint	26.75" x 26.75"	42.7" x 26.75"	74.5" x 26.75"
<b>NODE</b>			
Central Processor (CPU)	Intel 80286 (8 MHz) 16 MBytes physical addressing Memory management and protection		
Numeric Processor (NPU)	Intel 80287 (10 MHz) 32-, 64-, 80-bit floating point (IEEE 754) 32-, 64-bit integer 18-digit BCD operands		
Memory	512 KBytes dual-port RAM with byte parity, expandable to 4.5 MBytes of RAM 64 KBytes PROM monitor (expandable)		
Communication Channels	Eight total. Seven to nearest neighbor nodes via Intel's 82586 communication coprocessors and 1 Ethernet channel to Cube Manager via 82586/82501		
Communication Bandwidth	H/W: 2.5 MBytes/sec max.		
Control I/O	Reset, interrupt		
iLBX II Port	Bus bandwidth: 8 MByte/sec max. 16 MByte addressing 8- and 16-bit data transfers over 32-bit path Even numbered slots are masters; odd are slaves		
Indicators	Red LED Green LED		
Size	2 x 4 Eurocard (9.2" by 11") with two 96-pin male DIN connectors		

**Table 63. iPSC-VX System Specifications**

Vector System Feature	iPSC-VX/d4	iPSC-VX/d5	iPSC-VX/d6
Number of Nodes	16	32	64
Peak System Performance (MFLOPS)			
64-bit	106	212	424
32-bit	320	640	1280
Total System RAM Memory (MBytes)	24	48	96
Total Node-to-Node Communication Channels	32	80	192
Spare Boards			
Node Processors	0	1	2
Vector Processors	1	1	2
Cube Footprint (in)	26.75 x 26.75	42.7 x 26.75	74.5 x 26.75

**Table 64. Vector Processor (VP) Board**

Arithmetic Unit	<p>ALU: 100 nsec cycle time, pipelined operation  32-bit/64-bit floating-point (ADD,SUB)  32-bit integer (ADD,SUB,AND,OR,XOR)  Multiplier: 100 nsec (32-bit) cycle time or 300 nsec (64-bit) cycle time, pipelined operation  32-bit/64-bit floating point MULTIPLY</p>
Program Memory	<p>32 KBytes (4K x 64), 50 nsec static RAM  Directly loadable through iLBX™ II bus by 80286 node CPU  Supports VecLib function library and runtime monitor</p>
Data Memory	<p>1.0 MBytes (256K x 32), 250 nsec cycle time dynamic RAM  Dual ported, can be directly addressed by the VP's dedicated 32-bit Address ALU, or through the iLBX II bus by the 80286 node CPU (on a cycle stealing basis).    Extends the 80286 node memory space to 1.5 MBytes.  Used as a shared data workspace for the node CPU and vector processor.  Also available to the node CPU for user application code.</p>
Fast Data Memory	<p>16 KBytes (4K x 32), 100 nsec cycle time static RAM  Dual ported, can be directly addressed by the VP's dedicated 32-bit Address ALU, or through the iLBX II bus by the 80286 node CPU (on a cycle stealing basis). Used as high-speed data storage for table functions and intermediate computational results. 4 KBytes are reserved for a user scratch pad.</p>
Data Types	<p>IEEE 754 floating-point (except gradual underflow)  Single precision real: 32-bit  Double precision real: 64-bit  Single precision complex: 2*32-bit  Double precision complex: 2*64-bit  Integer/Logical: Supports 32-bit format of the 80286</p>
iLBX II Port	<p>Provides 80286 node CPU with 1 wait state memory mapped access to VP program and data RAM. Supports 8-, 16- and 32-bit accesses.</p>
Indicators	<p>System directed or user programmable red and green LEDs are viewable from the board's face plate or from the system's front panel display.</p>
Size	<p>2 x 4 Eurocard (9.2" by 11") with two 96-pin male DIN connectors. Includes data memory daughter board.</p>



**Table 65. Cube Manager Features**

<b>Cube Manager</b>	
Central Processor (CPU)	Intel 80286 (8 MHz)
Numeric Processor (NPU)	Intel 80287 (10 MHz)
Memory	2 MByte iLBX memory with ECC expandable to 6 MBytes
Mass Storage	140 MByte 5¼" Winchester disk 360 kByte 5¼" floppy disk (DS, DD) 45 MByte cartridge tape drive
MULTIBUS Expansion Slots (IEEE 796)	3 available slots at 0.6" spacing 1 reserved for iLBX memory, 2 for standard MULTIBUS 93 watts available power
Printer Port	Centronics compatible
User Processes Supported	50 (XENIX configuration parameter)
Global Channel	Ethernet (IEEE 802.3)
<b>Terminal</b>	<b>WYSE 75</b>
Compatibility	VT100, ANSI X 3.64
Character Set	7 x 13 matrix in 10 x 13 cell 128 ASCII character set Upper/lower case with line drawing graphics Cursor block or underline selectable, with or without blinking

**Table 66. Physical Specifications**

	<b>32-Node Unit</b>	<b>Cube Manager</b>	<b>Terminal</b>	<b>Keyboard</b>
Height	49"	6.5"	12"	2.25"
Width	16"	17"	12.3"	17.25"
Depth	16"	20"	13"	7.6"
Weight	200 lbs	40 lbs	12 lbs	2 lbs
Footprint	26.75" x 26.75"	17" x 20"	12" x 12.3"	17.25" x 7.6"

**Table 67. Electrical & Environmental Specifications**

	Each 32-Node Unit	Cube Manager	Terminal/Keyboard
<b>ELECTRICAL</b>			
AC Voltage	230 VAC $\pm$ 15%	115/230 VAC $\pm$ 10%	115/230 VAC $\pm$ 10%
AC Current	13.8 amps	5.8/2.9 amps	2/1 amps
Frequency	50/60 Hz $\pm$ 5%	50/60 Hz $\pm$ 5%	50/60 Hz $\pm$ 5%
Power	2704 watts 9226 btu/hr	367 watts 1320 btu/hr	45 watts 154 btu/hr
SAFTETY/RFI/EMI	UL 478	UL 114	UL
(designed to meet)	CSA C22.2 No. 154	CSA 22.2	
	VDE 0806	FCC Docket 20780	
	VDE 0871		
	IEC 380	IEC 435	
	FCC 47 CFRJ Class A	VDE 0871	
<b>ENVIRONMENTAL</b>			
Operating Temp.	10–35°C	10–35°C	0–50°C
Humidity	85%, max. non-condensing	20–80%	10–90%
Altitude	0–10,000 ft	0–8000 ft	0–15,000 ft
Acoustical	50 dBA, max		

## IPSC™ USER TRAINING

Training for one customer staff member is included with the purchase of each iPSC system. This 5-day course titled “Programming Concurrent Computers” provides students with the fundamental knowledge, strategies, skills and tools needed to design and implement large-scale concurrent software for the iPSC system.

## SOFTWARE SUPPORT

Intel provides the following software support during the warranty period and under annual software support contract after warranty. Further details are described in iSC’s Terms & Conditions of Services.

## ORDERING INFORMATION

For more information on the Intel iPSC concurrent computer family, contact:

Intel Scientific Computers  
 15201 N.W. Greenbrier Parkway  
 Beaverton, Oregon 97006  
 (503) 629-7629

## SOFTWARE

Intel offers an extensive selection of operating systems, high level languages, development and debug support that is specifically tuned for microcontrollers, microprocessors, and microcomputer-based boards and systems. Intel also maintains the INSITE Library of user software. Intel publishes a Development Tools Handbook, a comprehensive directory of tools available directly from Intel.

### DEVELOPMENT SOFTWARE

(For information on development systems and debuggers, see the Development Tools section, page 20.)

Intel provides a range of microprocessor development software, from assembly to high level languages. This software is available for a wide range of development environments.

**Table 68. Development Languages and Utilities**

Product	Description
Assemblers	All Intel assemblers are strongly typed and provide full macro support.
Utilities	Linkage utilities allow independent assembly/compilation of modules. Library managers allow the management of standard modules and routines. In the case of the iAPX 286 (protected mode), a system builder is provided to allow easy configuration of a complex protected/memory managed systems. Locate utilities allow modules to be assigned absolute memory addresses and thus easily loaded into ROM.
PL/M	PL/M was the first high level language expressly designed for microprocessors. PL/M is a procedure-oriented language with data structuring facilities and gives the engineer full control over microprocessor-dependent features. It is one of the most widely used tools in the microprocessor and embedded controller world.
PASCAL	PASCAL is a superset of ISO-PASCAL. Extensions include independent compilation and port I/O. In addition, PASCAL embodies the most advanced code optimization techniques to achieve extremely efficient programs.
FORTRAN	FORTRAN is an ANSI-77 standard compiler. Among its features are full 8087 support and the ability to handle very large arrays.
C	C is a true implementation of the "C" programming language as defined by Keringhan and Ritchie. C is a high level language offering flexibility and portability of programs.

The following table shows the software tools available for specific Intel microprocessors on Intel host systems and non-Intel computers.

**Table 69. Intel Language/Host Summary**

Language	Component Family	Host Code
Macro Assembler + Utilities	MCS-51 Family MCS-96 Family 8086 Family 80286 (Protected Mode) 80386	1,2 1,2 1,2,3,4 1,2,3,4 1,3,4
PL/M	MCS-51 Family MCS-96 Family 8086 Family 80286 (Protected Mode) 80386	1,2 1,2 1,2,3,4 1,2,3,4 1,3,4
PASCAL	8086 Family 80286 (Protected Mode)	1,2,3 1,2
FORTRAN	8086 Family 80286 (Protected Mode)	1,2,3 4
"C"	8086 Family 80286 (Protected Mode) 80386	1,2,3 1,2,3,4 1,3,4
Ada (Reference Sell)	8086 Family 80286 (Protected Mode)	3,4 3*

**NOTE:**

\* = Planned

++ VAX, MicroVAX and VMS are trademarks of Digital Equipment Corp.

**Host Codes**

1 = PC XT or AT running DOS 3.0 or greater

2 = Intel 8086 Family Basic System (e.g., MDX Series IIIE, RMX -86)

3 = VAX++/VMS Minicomputer VAX, MicroVAX++/VMS Minicomputer

4 = Intel 80286 (Protected) Basic System (e.g., RMX286 or XENIX 286)



## **INSITE™ User's Library**

INSITE is a collection of programs that have been written by users of Intel microcomputers, single board computers, and development systems. These programs are available on paper tapes, diskettes or source listings and includes monitors, conversion routines, peripheral drivers, translators, math packages and even games. The library can also serve as a learning tool for users unfamiliar with assembly or high level languages associated with Intel's microprocessors.

## **OEM SOFTWARE**

Intel offers a broad range of OEM operating systems and languages. For real-time, embedded and commercial applications, the iRMX™ Operating System family is the OEM software offering. The iRMX 86 Operating System is the entry level family member supporting a broad range of Intel processors, making it the current world standard for 16-bit applications requiring fast response times to real time events. The newest family member, the iRMX 286 Operating System is the evolving flagship 16-bit iRMX family member for the late 1980s.

Intel also supports XENIX 286 R3.0, a fully licensed version of UNIX tuned especially for Intel's System 310 and other microcomputers. XENIX is well suited to development and business applications. In addition, Intel provides a set of high-level languages and applications packages for the XENIX operating system. Many of these packages are sold by Intel to provide single stop shopping for system customers. Also, Intel's microprocessor and microcontroller are supported by a set of high-level languages: PL/M, C, Pascal and FORTRAN and assemblers (refer to the Development Systems section).

The OpenNET software products, which currently include iRMX Networking software, XENIX Networking software and the iNA 960 Transport Software are based in industry standard networking protocols and provide transparent interoperation between XENIX, iRMX and PC/DOS or MS/DOS systems.

## **iRMX™ OPERATING SYSTEMS**

The iRMX Operating System family is easy-to-use, real-time, multi-tasking and multi-programming software developed to provide OEMs standard off the shelf operating system services. These services manage and extend the resources of the appropriate hardware facilities. The iRMX 86 system manages the resources of iSBC 86/88/186/188 and 286 (real address mode) Single Board Computers as well as other 8086, 8088, 80186, 80188 and 80286 (real address mode) based microcomputers. The iRMX 286 system manages the resources of iSBC 286 (protected address mode) Single Board Computers as well as other 80286 (protected address mode) based microcomputers. Both the iRMX 86 and iRMX 286 systems are available in user configurable software packages and fully integrated into the System 286/3XX families of Microcomputer Systems. These Operating Systems provide a number of standard interfaces that allow iRMX Applications to take advantage of industry standard device controllers, hardware components, and a multitude of software packages developed by Independent Software Vendors (ISVs).

## **XENIX\* Operating System**

Intel offers the XENIX 286 R3.0 Operating System specially configured and optimized for the System 310AP supermicro system. XENIX 286 R3.0 for the 80286 is a fully licensed and enhanced version of UNIX\*\* System III that has been codeveloped by Microsoft Corp. and Intel Corp. This is a multi-user, multi-tasking memory protected operating system that utilizes the features of the 80286 and 80287 to provide a high performance

\*XENIX is a trademark of Microsoft Corp.

\*\*UNIX is a trademark of Bell Labs.

cost effective UNIX engine. The integration of operating system features onto the 80286 chip also provides an unparalleled amount of software compatability between different machines running the XENIX Operating System. Intel's product engineering, evaluation, documentation and support groups are involved to insure that the software has been thoroughly tested for reliability and ease of use by systems builders.

**Table 70. Operating Systems**

<b>Feature</b>	<b>iRMX™ 86</b>	<b>XENIX* 286</b>
<b>PRIMARY FEATURES</b>		
Multitasking Support	Yes	Yes
Device Driver Support	Yes	Yes
File System Support	Yes	Yes
Optional Multiprocessing Support	Yes	Yes
Any Combination of PROM and RAM residency	Yes	No
Building-block approach	Yes	Yes
Multiprogramming Support	Yes	Yes
Interactive Support	Yes	Yes
On-target Development	Yes	Yes
<b>ADVANCED FEATURES</b>		
Hierarchical directories	Yes	Yes
Custom device drivers	Yes	Yes
Low-overhead random access support	Yes	Yes
File access control	Yes	Yes
Automatic buffering	Yes	Yes
Load-time location	Yes	Yes
Utility commands	Extensive	Extensive
Interactive debugger	Yes	Yes
Interactive configuration	Yes	No
Communications/Networking	Yes	Yes
Text Processing	Yes	Yes—Extensive
Source Code Control System	No	Yes

## **iRMX™ Languages and Utilities**

The Intel iRMX languages and utilities provide full “on-the-target-system” software development capability for the 86/300 and 286/300 families of microcomputer systems and iSBC 86/88/186/188/286 or 86/88/186/188/286 based systems. This facility allows OEMs to allow their end users to make on-the-spot modifications and add additional capability to their applications. All languages are compatible with Intel's Universal Development Interface (UDI) “software bus”.

The iRMX languages run only on iRMX 86 or iRMX 286 but are fully compatible with Intel's software development languages allowing users to develop programs on Intel's Development Systems and then easily move it to an iRMX system.

The iRMX languages allow OEMs to select the correct language for their application. For technical applications, FORTRAN or Pascal can be used, for systems programming use PL/M; commerical—Pascal; and for size optimization—Macro Assembler can be used.

The iRMX utilities provide all necessary software for development.

**Table 71. iRMX™ Languages and Utilities**

Product	Description	Applicable Standard
iRMX 286 UTILITIES (R286 ASM 86)	EDIT is a powerful line oriented editing facility. BIND connects object modules which have been individually compiled into a single, relocatable object module. BUILD maps the relocatable object code into the 80286 memory segments. LIBRARIAN allows creation of object module libraries.	N/A
iRMX 286 PL/M (R286 PLM 286)	PL/M compiler which provides users with a powerful, microcomputer oriented system programming language. iRMX 286 PL/M is a compatible superset of PL/M 86 offering easy portability of software.	Intel PL/M
iRMX 86 C (RMX 866)	C compiler which provides users with high level language offering flexibility and portability of programs.	Kernighan and Richie 1978
iRMX 86 BASIC (RMX 865)	BASIC interpreter which provides BASIC program generation.	N/A
iRMX 286 SCREEN EDITOR (R286 EDI 286)	A screen editor which provides users with a menu driven text-editor. By keeping the menu of commands always in view, even infrequent users of the editor are able to edit text quickly.	N/A

## **XENIX\* Languages and Applications**

Intel provides a set of high level languages and applications packages for the XENIX Operating System. Many of these packages are sold by Intel to provide single stop shopping for system's customers. Due to the need for a wide variety of software for a commercially oriented system. Intel also runs an active third party software program that provides systems, support and marketing assistance to third party developers who sell the resulting products directly to Intel OEMs. Please see the Database Products section for a description of the available, Intel supplied applications software.

**Table 72. XENIX\* Languages and Applications**

Product	Description	Applicable Standards
XENIX 286 C Compiler	Included with the XENIX 286 Operating System. High performance compiler for the C programming language tuned for the 80286. Provides full implementation as per Kernighan Ritchie book along with extensive type checking and error handling, 80287 floating point support and large model segmentation support.	—
XENIX 286 FORTRAN	See Development Software section for description.	ANSI 77
XENIX 286 BASIC	Industry standard Microsoft BASIC Interpreter provides interactive development and execution of the most popular dialect of the BASIC language.	ANSI x3.60 1978 Subset
XENIX 286 COBOL Compiler (XNX2867) and Run-time Incorporation Fees (XNX2868)	Offering of Microfocus COBOL, a mainframe caliber package for ANSI 1974 programs. Supports easy migration of existing programs (through support of standard), easy program development (through interactive environment and FORMS II visual programming tool) and cost effective pass through (using lower cost run-time only package for volume shipments).	ANSI x3.23 1974 to Federal High Level
XENIX 286 PL/M	See Development System Section for description.	—

\*XENIX is a trademark of Microsoft Corp.



**Table 73. OEM Operating Systems and High Level Languages**

Operating Systems	Languages Supported	Components <sup>(1)</sup>	MULTIBUS <sup>®</sup> (2) Boards	Systems <sup>(3)</sup>
iRMX 86	Assembler PASCAL 86/88 FORTRAN 86/88  BASIC-86 Interpreter C-86 PL/M 86	8086, 8088 80186, 80286 Family	iSBC 86/05 iSBC 86/12A iSBC 86/14 iSBC 86/30 iSBC 86/35 iSBC 88/25 iSBC 88/40 iSBC 186/03 iSBC 286/10A iSBC 286/12	86/380 86/310 286/380 286/310 310AP
iRMX 286	Assembler PL/M 286	80286	iSBC 286/10A iSBC 286/12	286/310 286/380 310AP
XENIX 286 R3.0 licensed version of UNIX System III	C language FORTRAN Cobol BASIC Interpreter	80286 Family PL/M	iSBC 286/10A iSBC 286/12	310AP

**NOTES:**

1. See Microprocessor Section on Page 12.
2. See Single Board Computer Section, Page 81.
3. See OEM Systems Section, Page 96.

## OpenNET™ Software Products

iNA 960 and its derivative iNA 961 implement the industry standard ISO 8073 transport protocols and provide reliable end-to-end message delivery between two networked systems on an IEEE 802.3/Ethernet or an IEEE 802.4 Token Bus LAN. iNA 960/961 is fully supported by Intel's IEEE 802.3 and IEEE 802.4 LAN hardware modules.

The iRMX Networking Software (iRMX-NET) and XENIX Networking Software (iXNX-NET) products are based on the Network File Access protocols developed by IBM, Microsoft and Intel and provide transparent remote file access between XENIX, iRMX and PC or MS DOS based systems. Transparent remote file access enables the user to work with remote files across the local area network as if they were local. iRMX-NET and XENIX-NET are supported by iNA 960 and Intel's LAN hardware modules. This first set of products run initially in IEEE 802.3 environments. In Q286 MAP Networking Software (MAP-NET™) will be available and will include FTAM, CASE, SESSION and run initially in the IEEE 802.4 environments.

The Intel OpenNET hardware and software products combined support all seven layers of the ISO Open Systems Interconnect Model.





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